

MS-7676

UATX Ver:10

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4106

HD Audio Codec:RTL892

LAN:RTL 8111E 10/100/1000

SIO:FIN71889AD

Flash ROM: 64 Mb SPI (PCH)* 2

Main Memory:

DDR3 (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UPI6234 (6+2-Phase)Dr.MOS

CPU+GPU

Controller:uP6113 Dr.MOS

CPU VTT CPU SA

Controller:uP6103A

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

SATA3.0X1 + e-SATA X1(MARVELL)

USB2.0 RearX4 Front x8(PCH)

USB3.0 RearX2 (NEC uPD720200)

1394 Controller - VT6315N-CE

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

on BOARD BUZZER

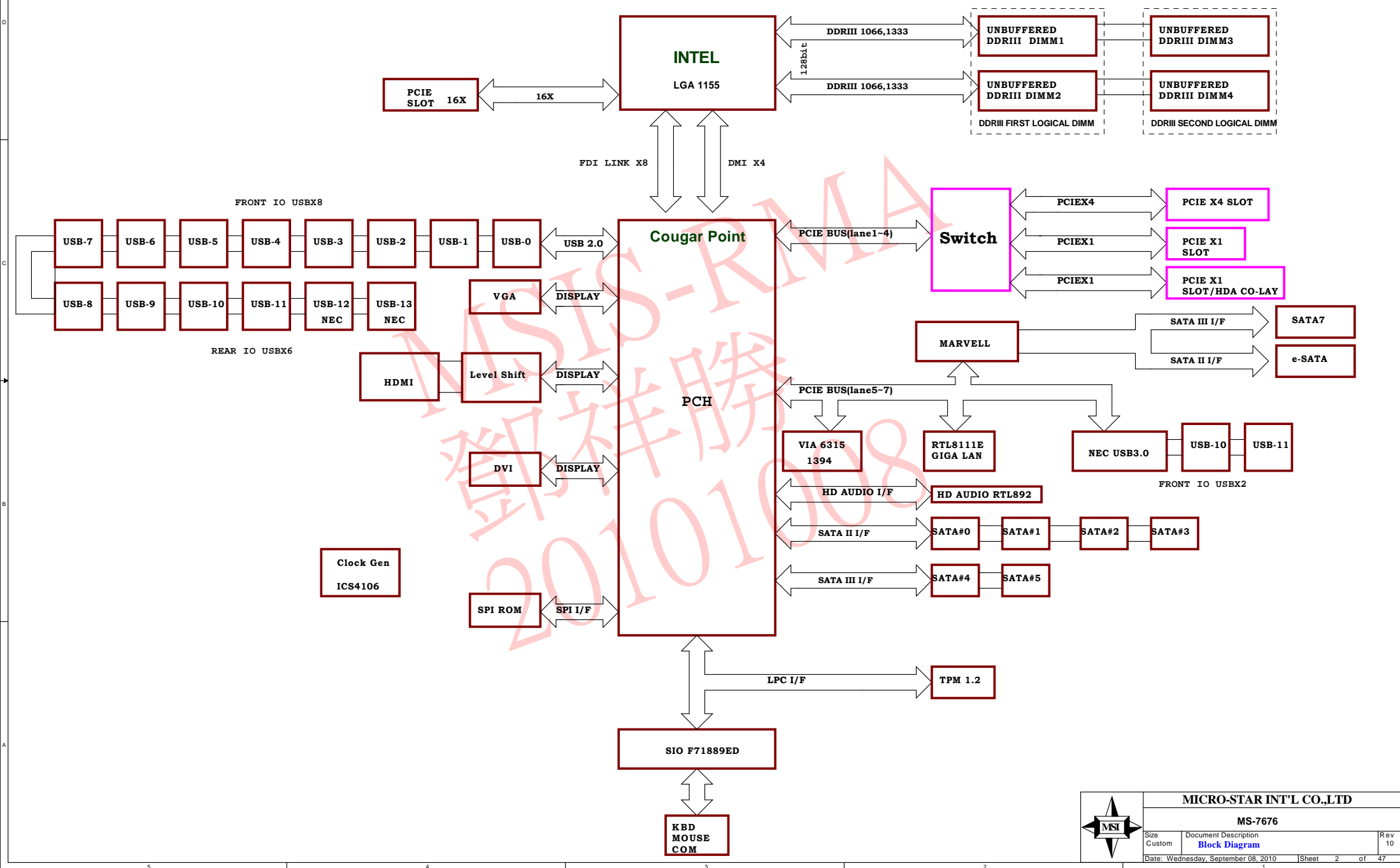
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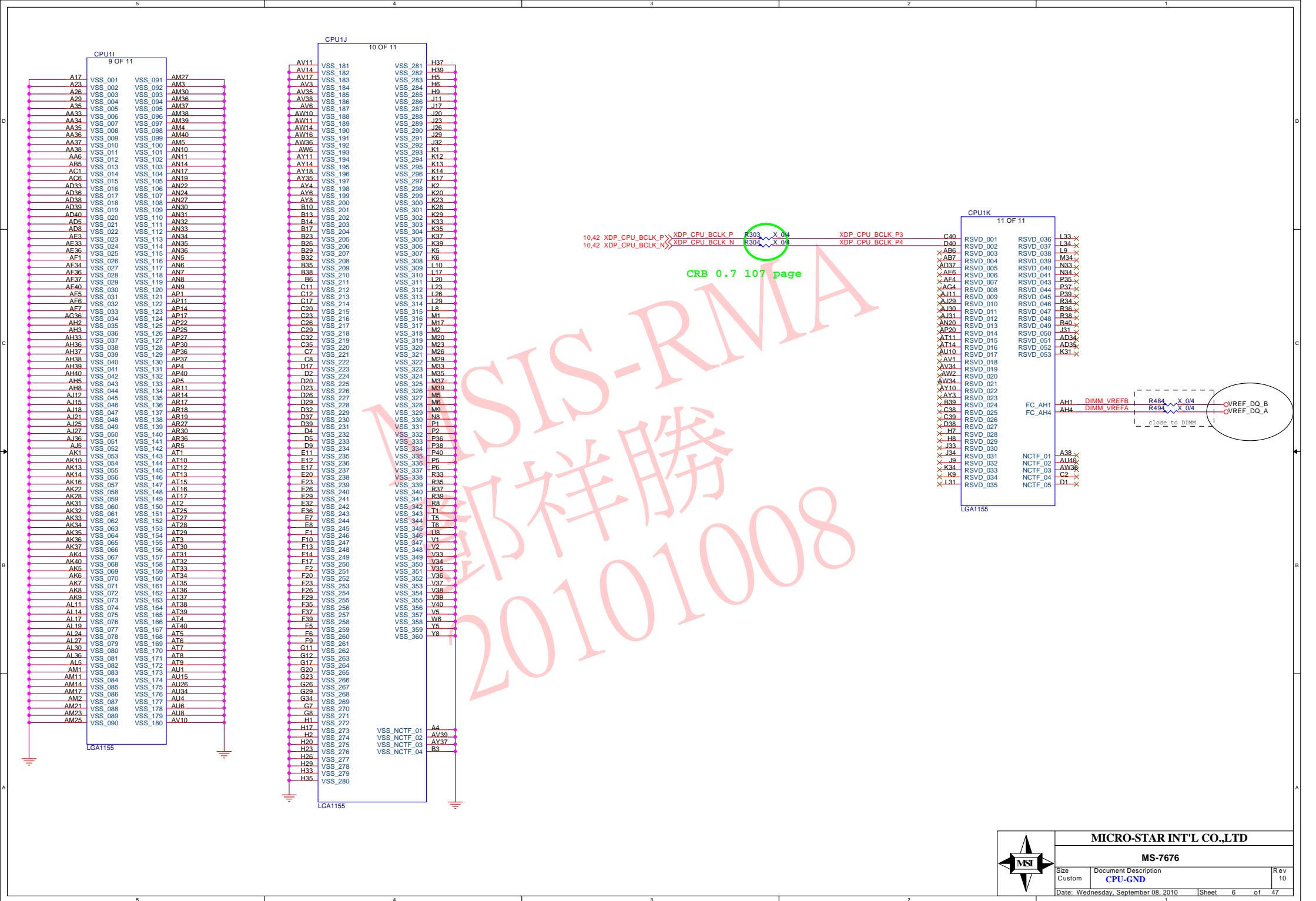


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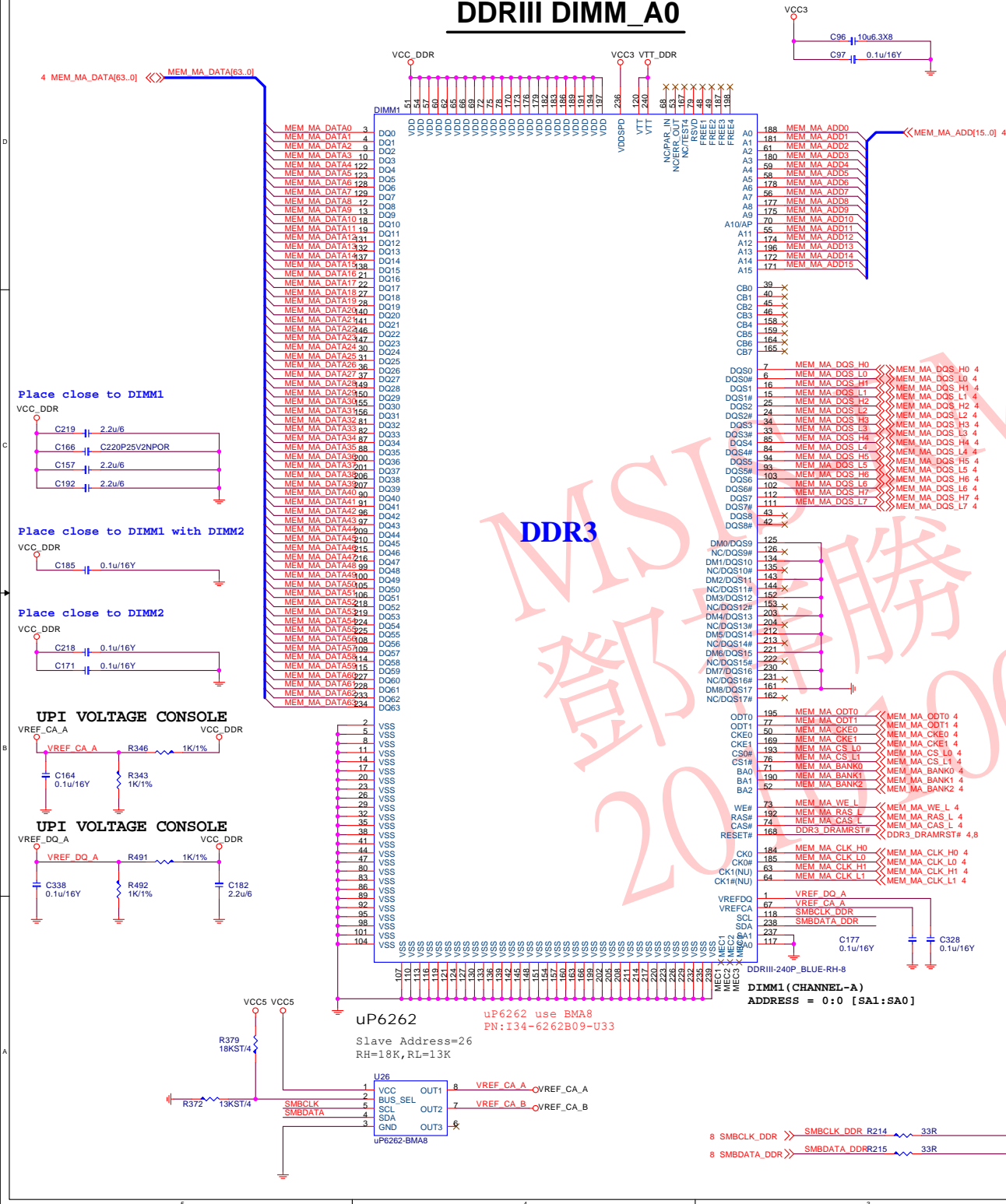
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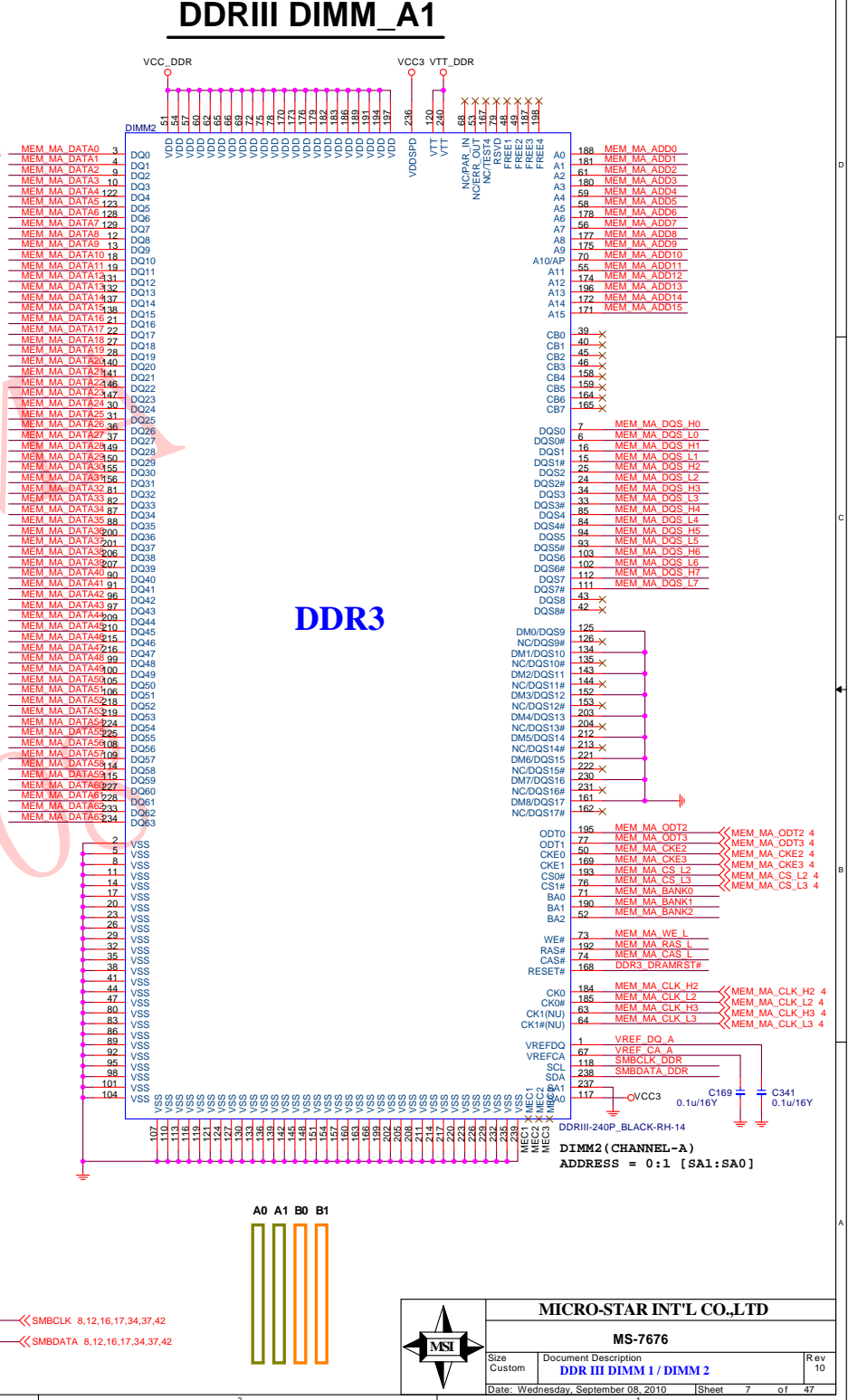




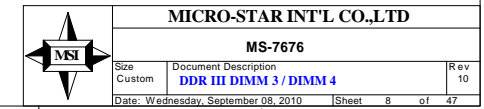
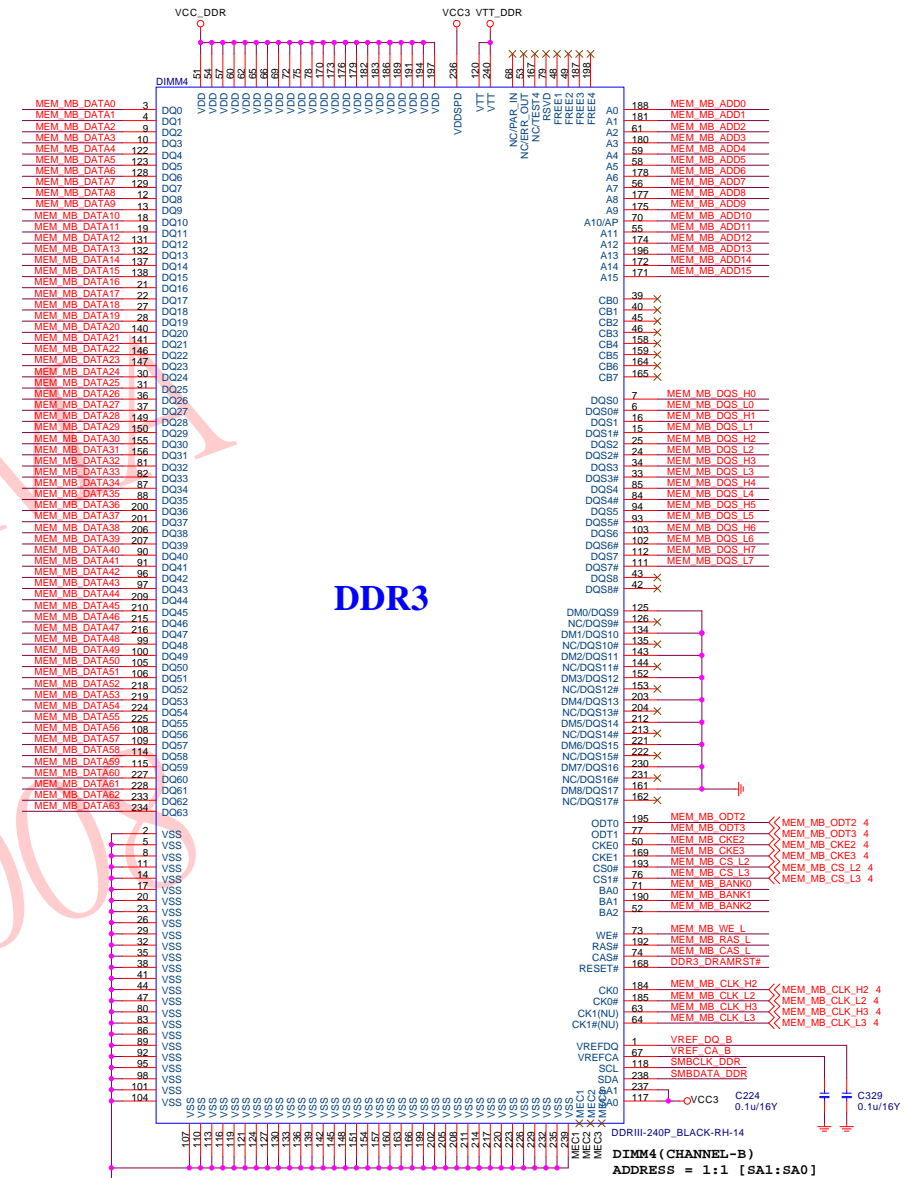
DDRIII DIMM_A0



DDRIII DIMM_A1



DDRIII DIMM_B1



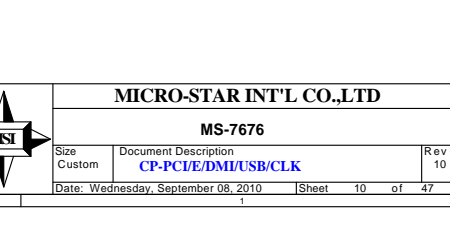
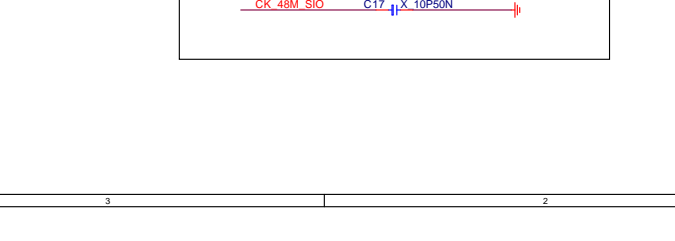
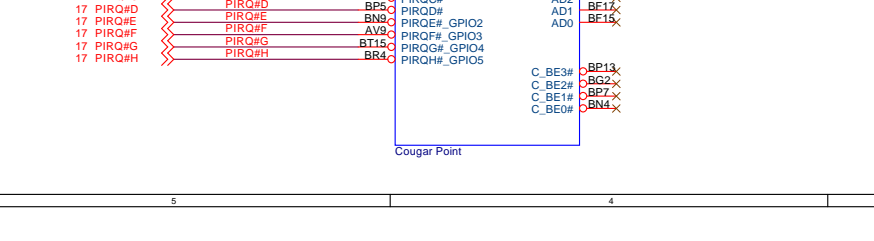
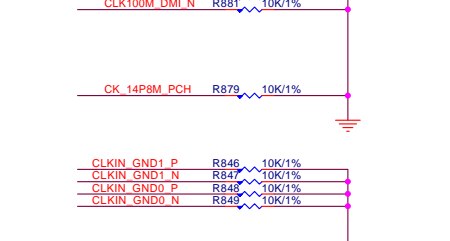
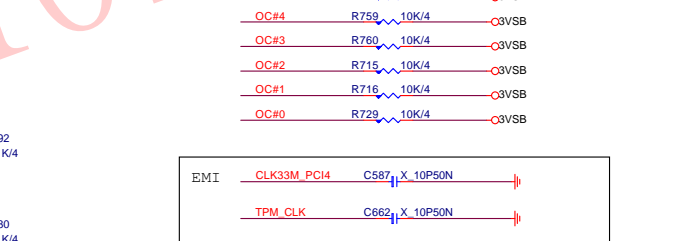
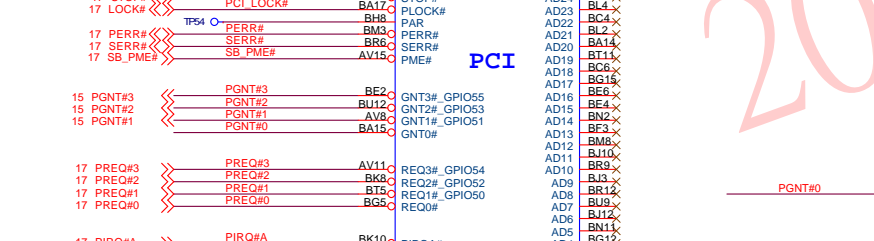
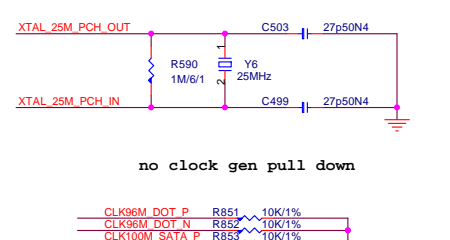
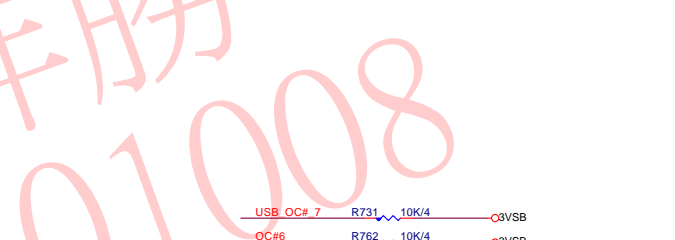
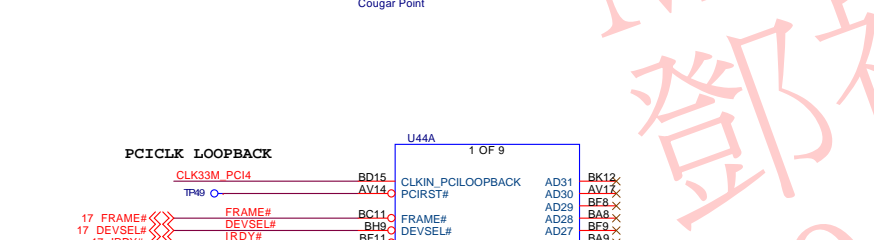
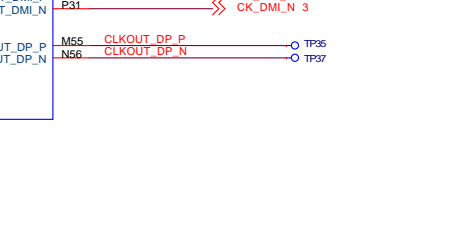
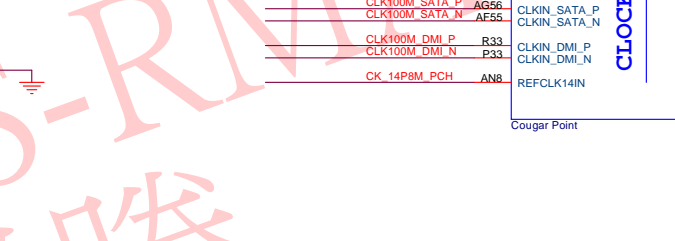
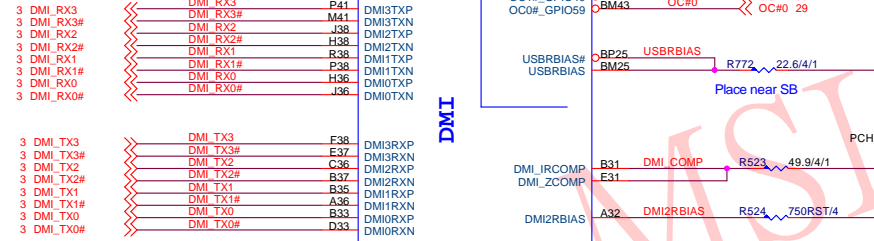
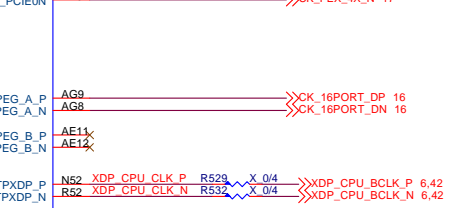
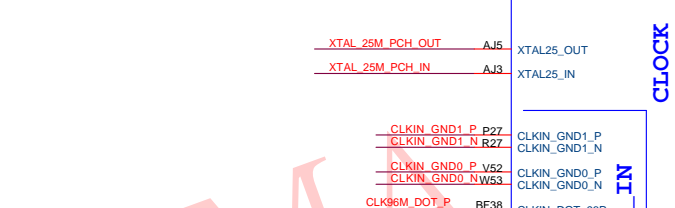
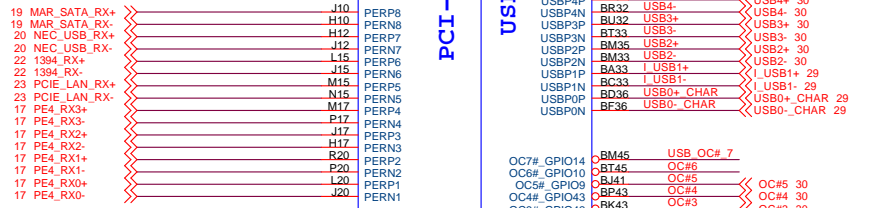
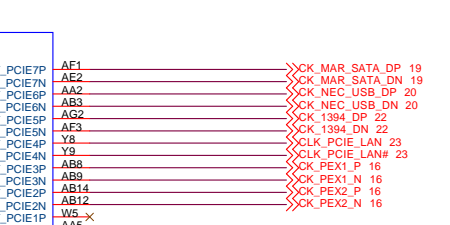
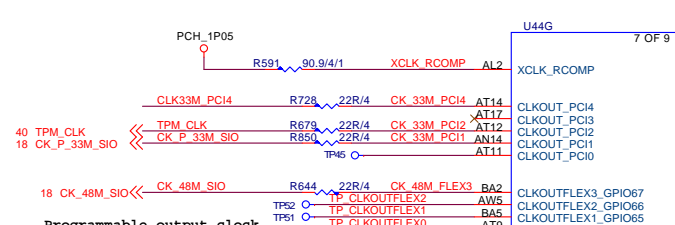
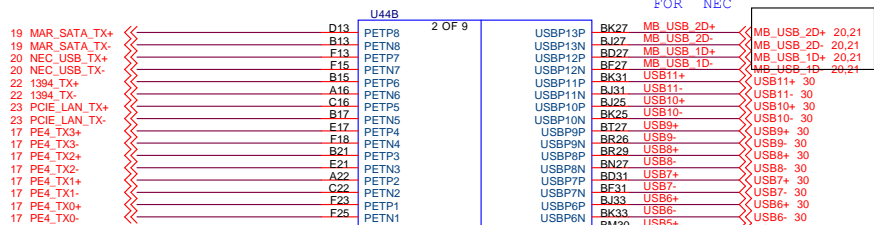
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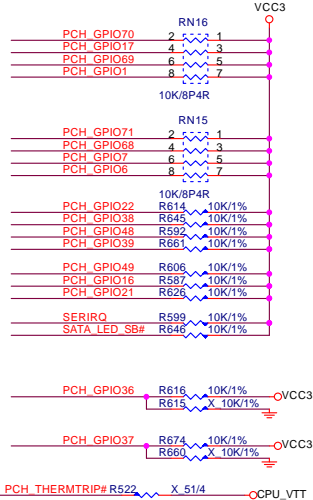
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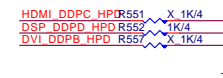


Pull HIGH for PCH

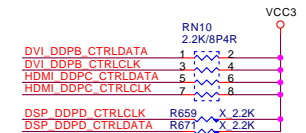


Close to PCH within 250 mils.

No VGA(pull down)



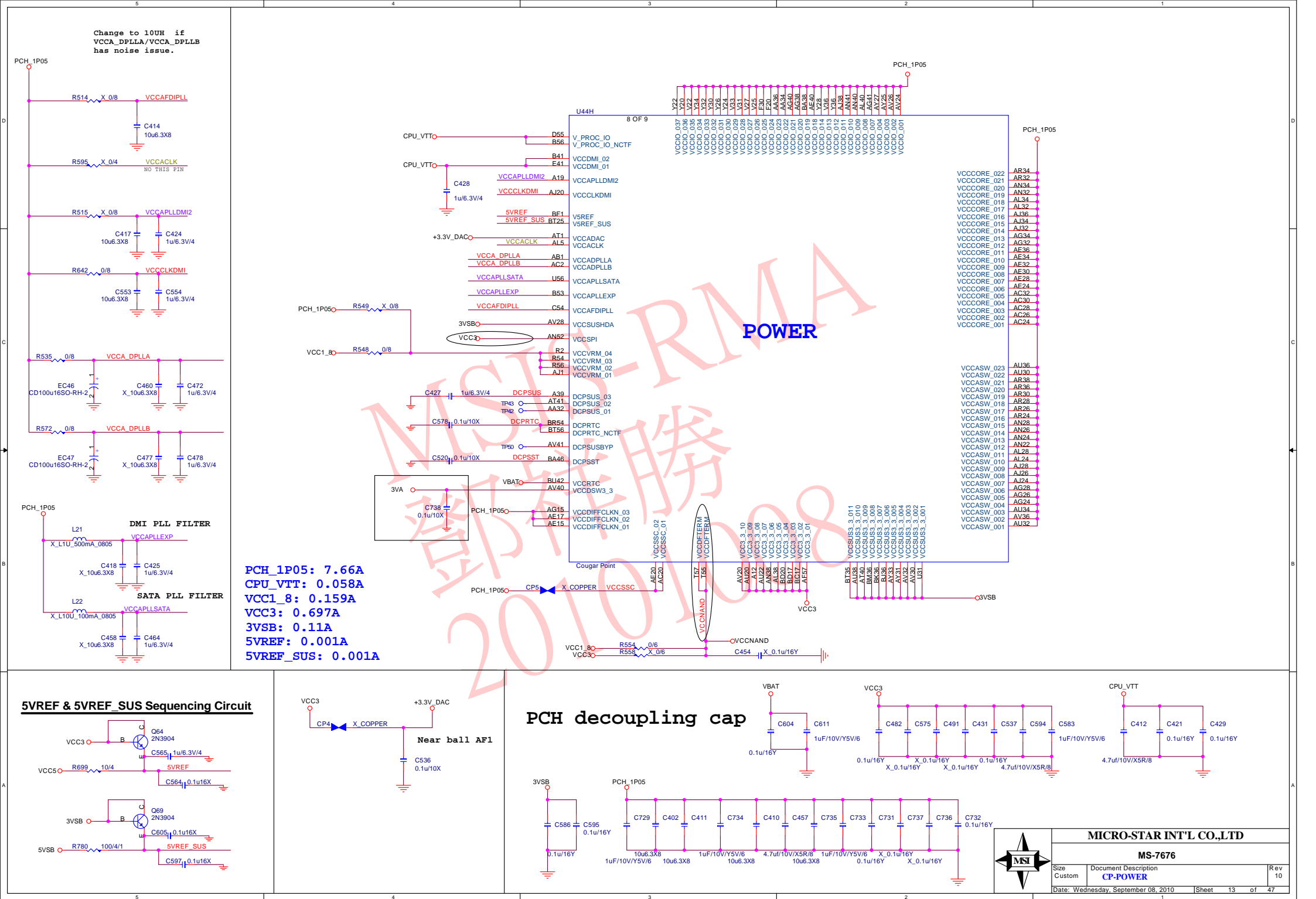
Enable VGA(CTRLCLK/DATA Pull High)



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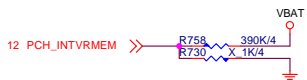
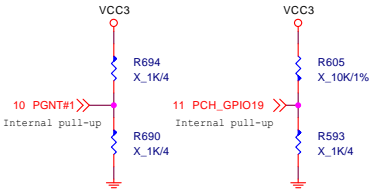
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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



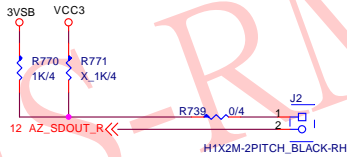
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



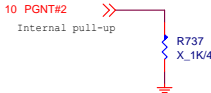
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

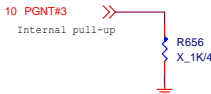


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

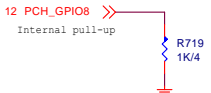
HDA_SDO has internal pull down. Default should be connected to SDIN of codec, no pull up/down. To Disable ME need to have a jumper to pull high



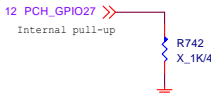
DMI AC/DC MODE
0 : AC
1 : DC *



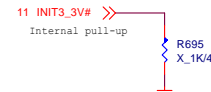
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

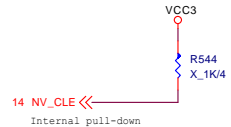


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

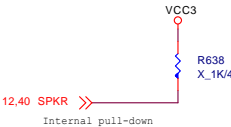


INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

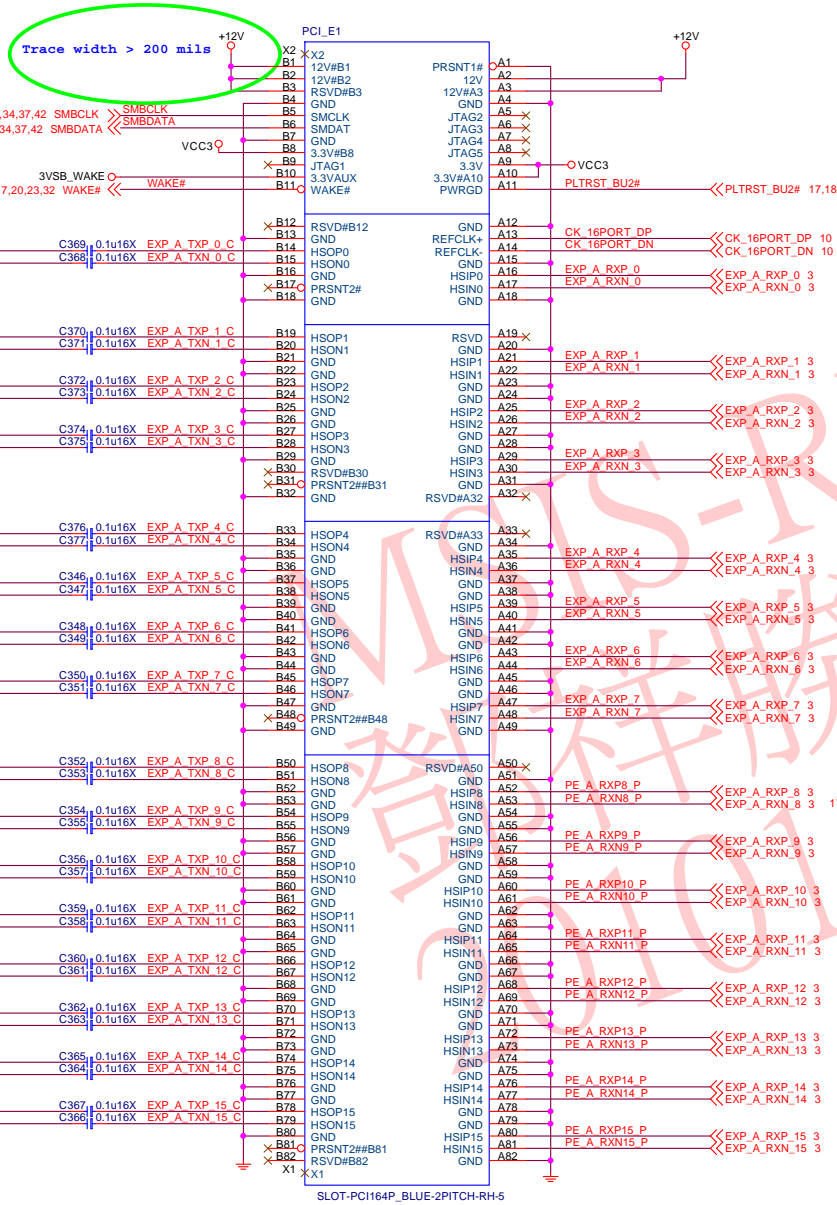


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

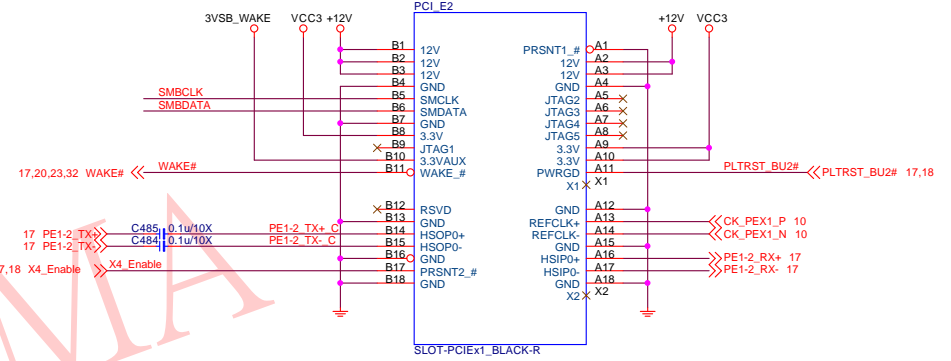


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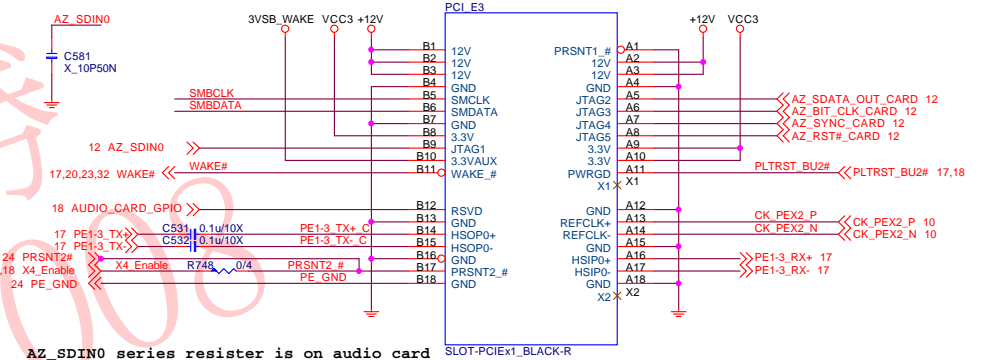
PCI_Express X16 slot



PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT

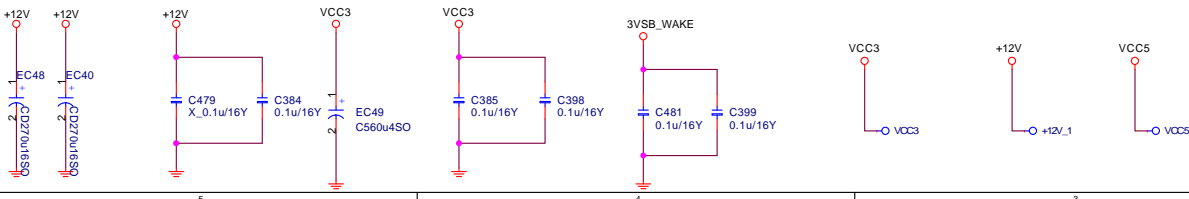


AZ_SDIN0 series resistor is on audio card

AUDIO_CARD_GPIO

HI:LED OFF

LOW:LED ON

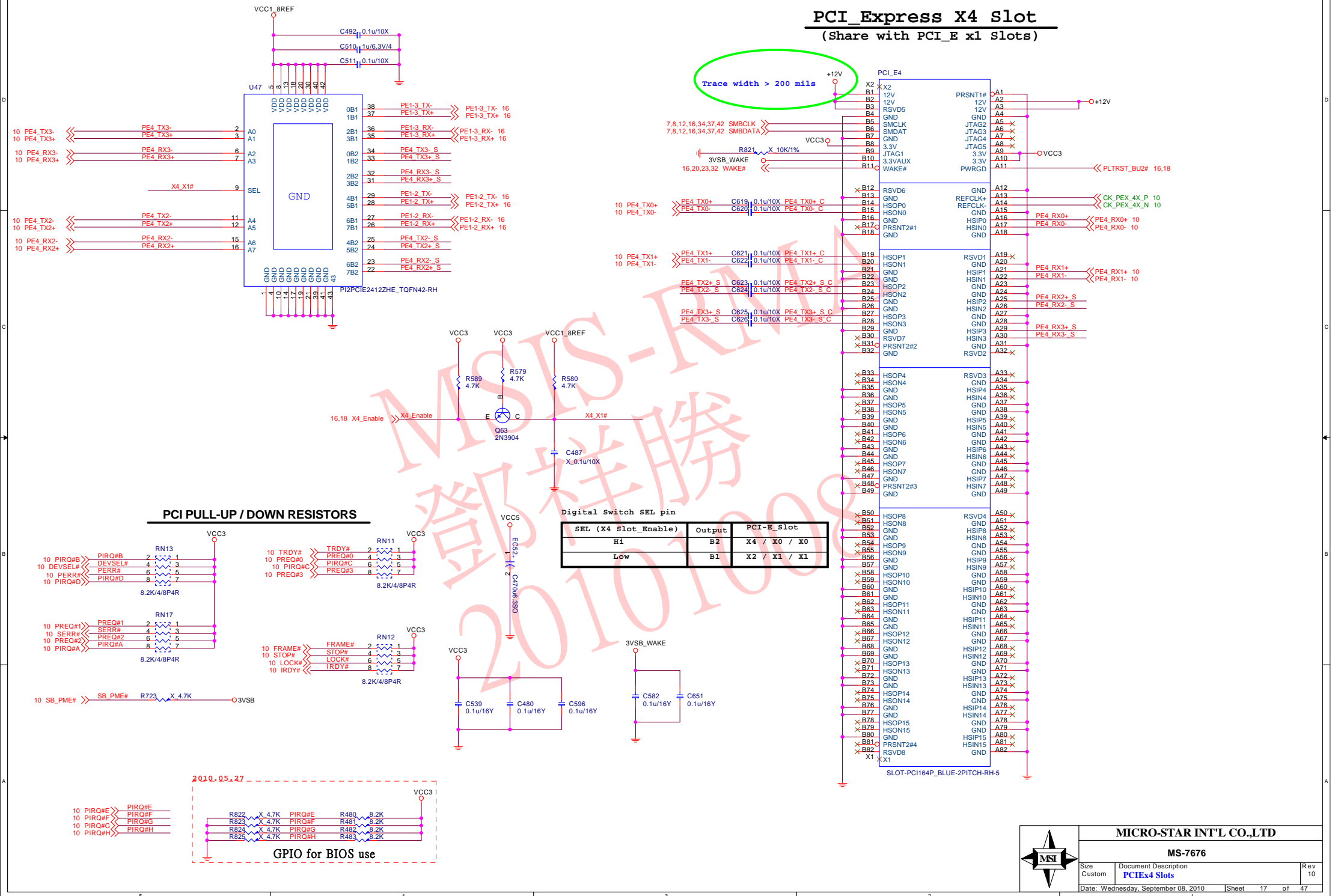


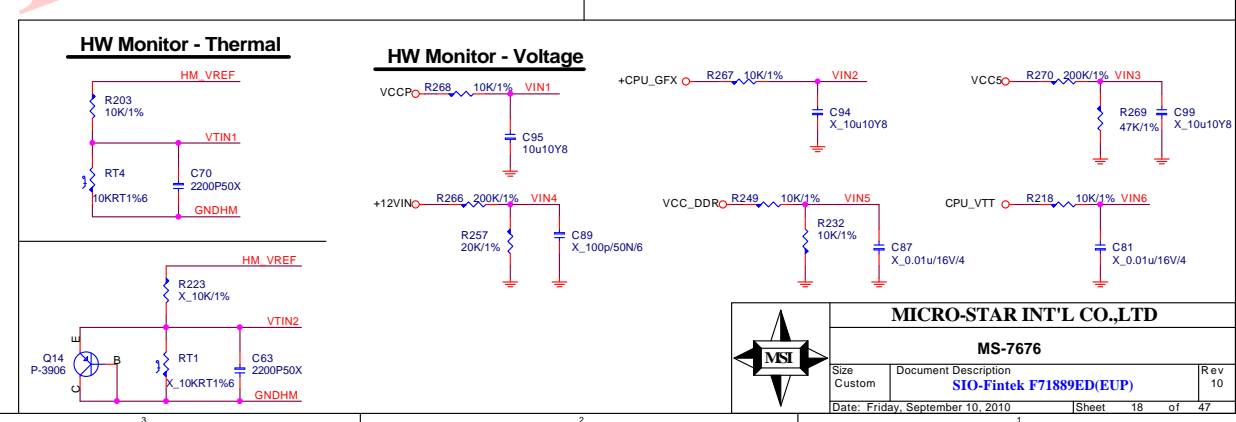
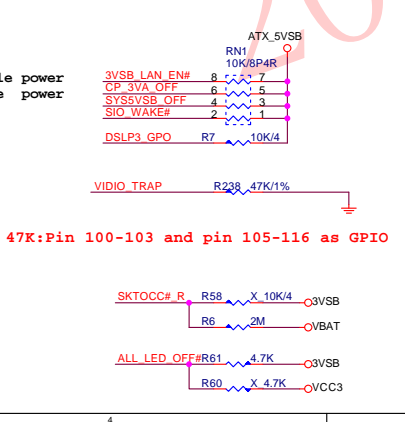
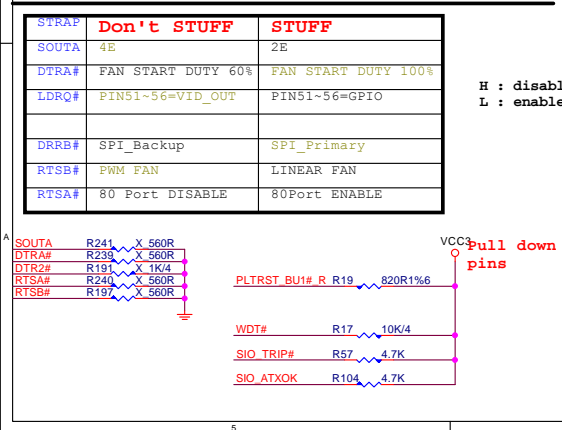
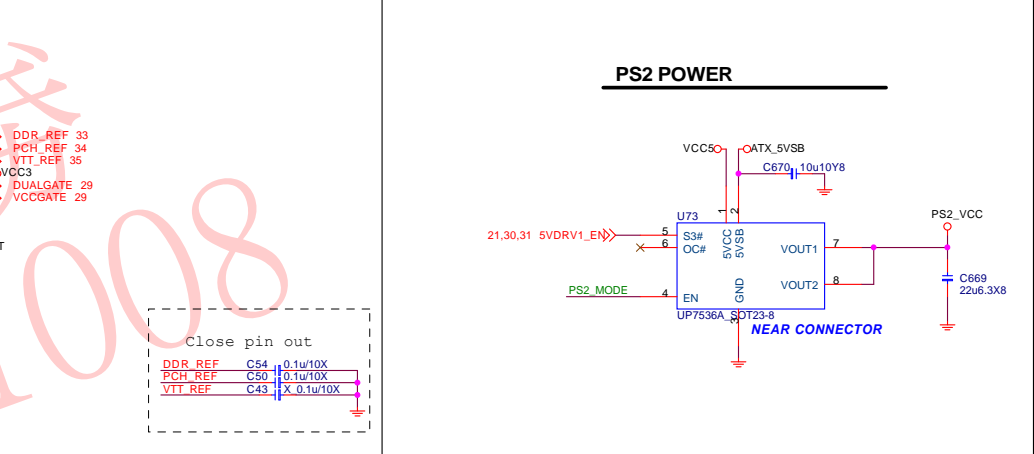
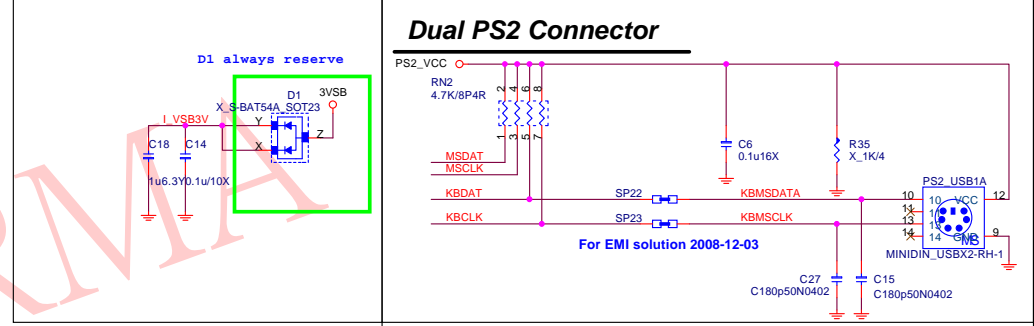
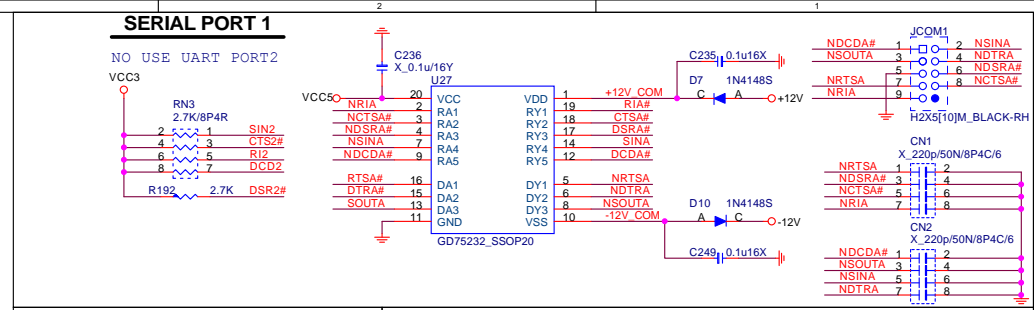
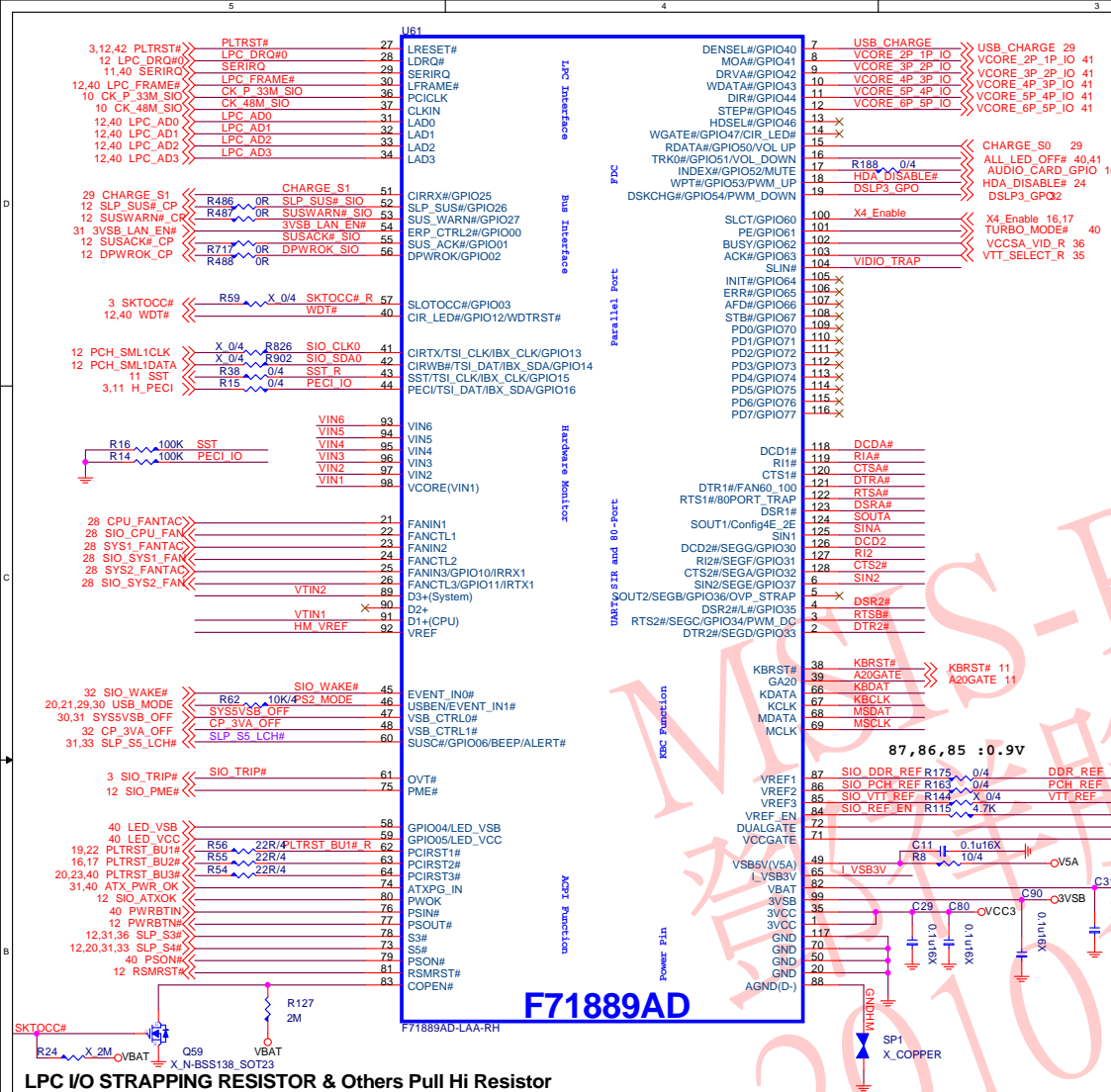
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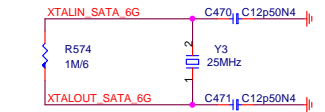
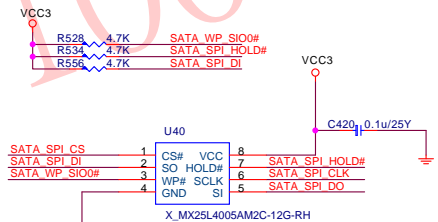
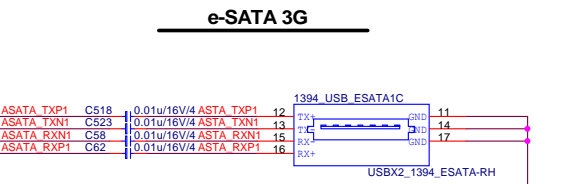
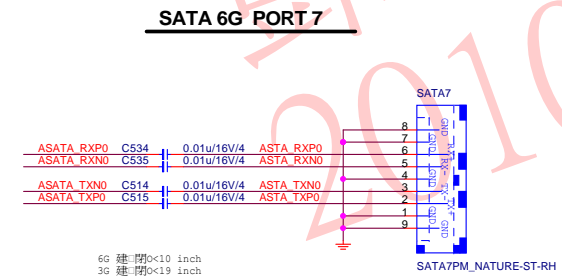
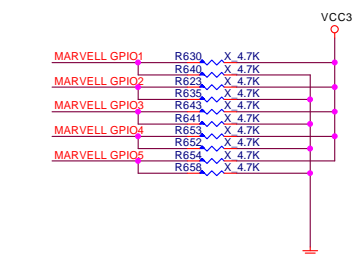
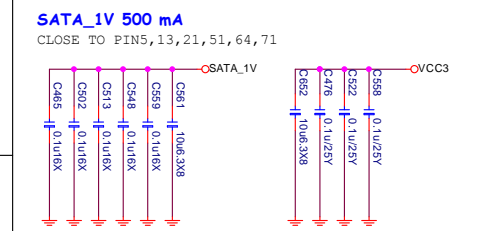
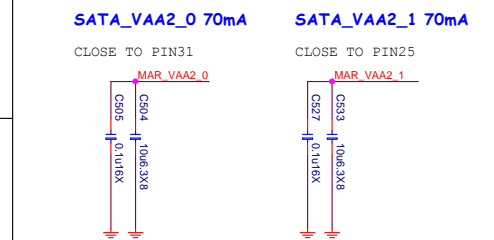
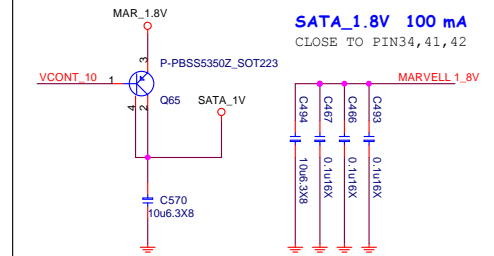
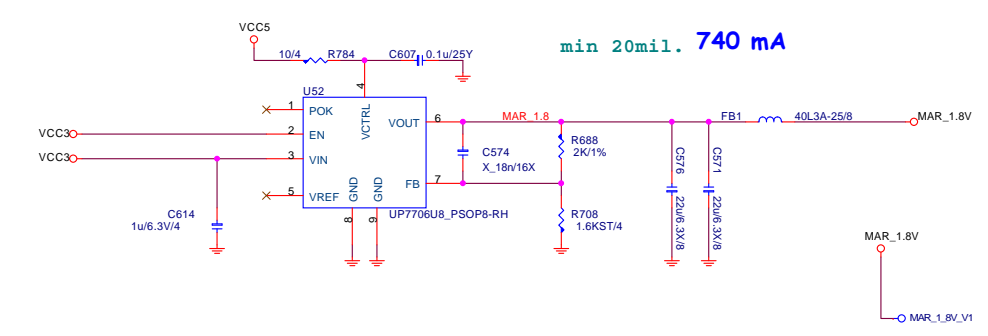
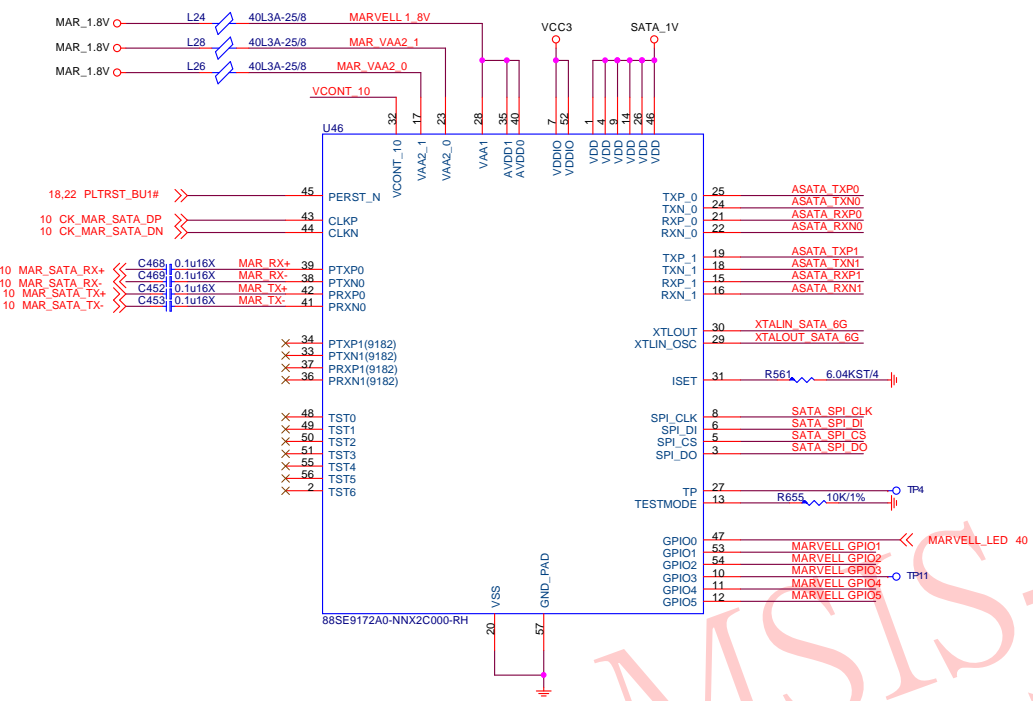
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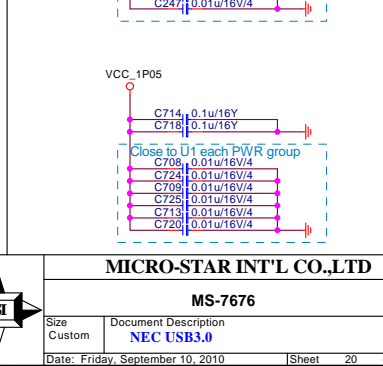
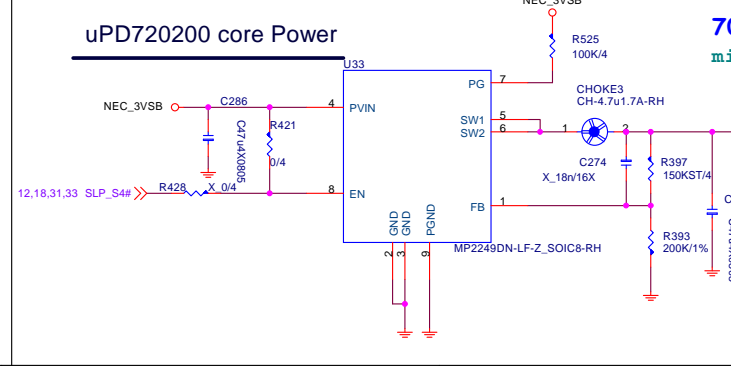
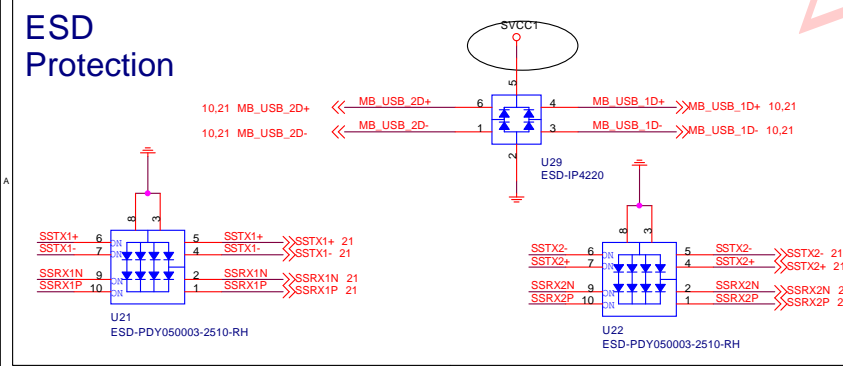
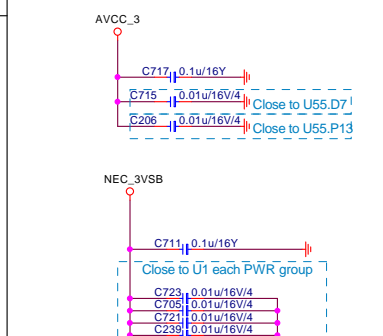
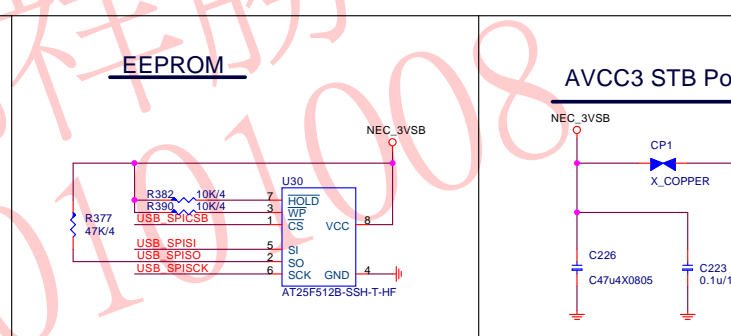
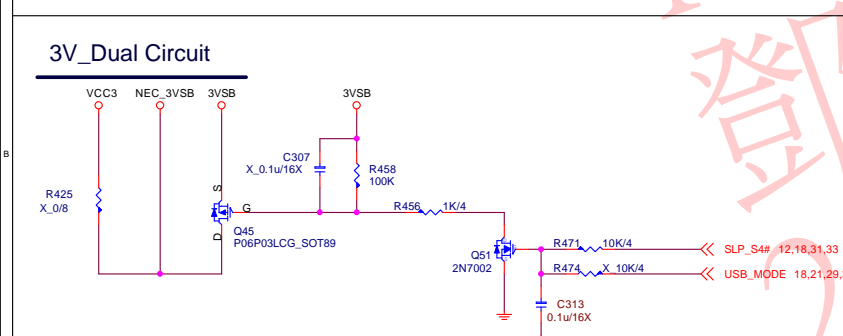
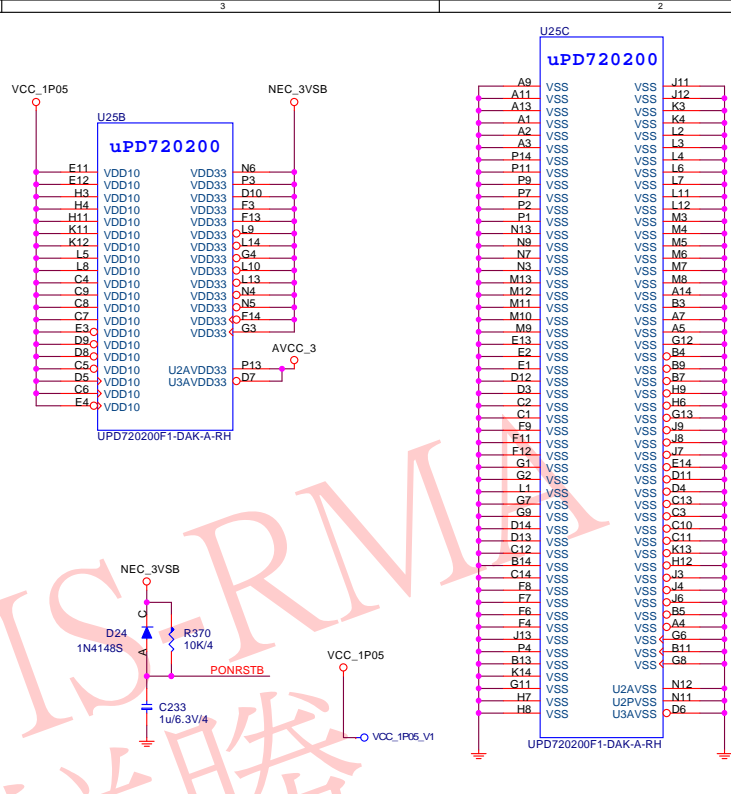
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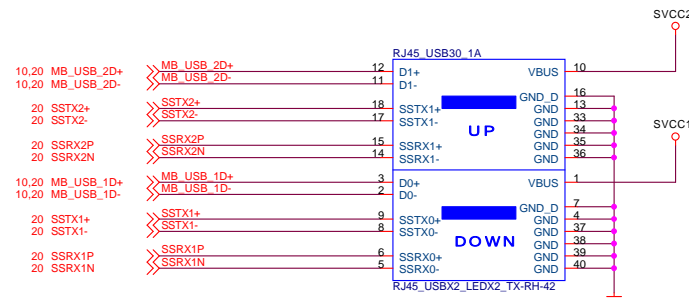
PCI Express X4 Slot (Share with PCI_E x1 Slots)



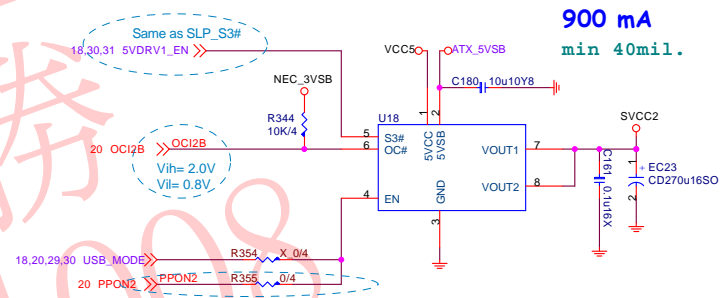
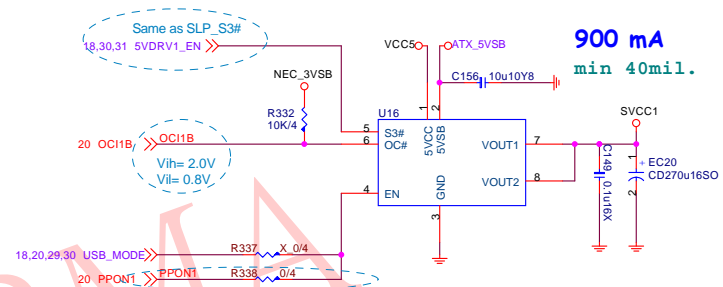








All power sources of uPD720200 are supplied, PPNx is enable.
PPONx is low when OCix going to low.

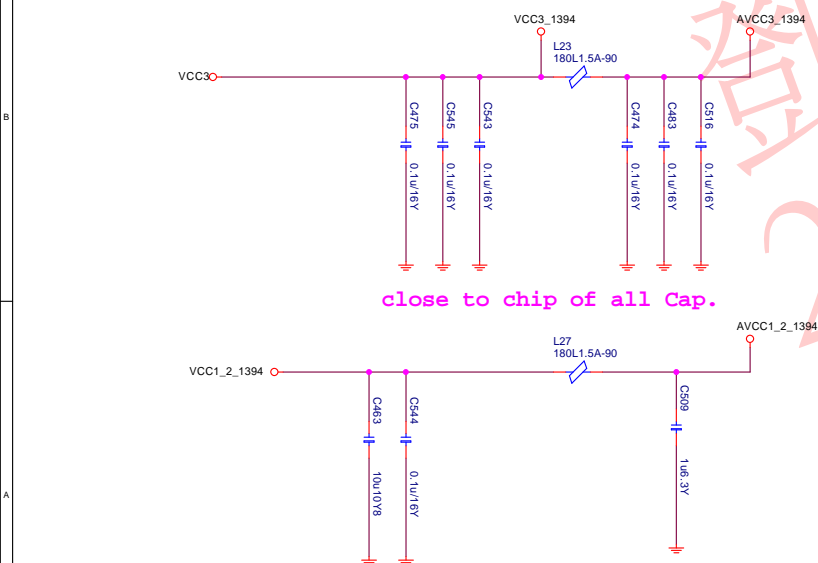
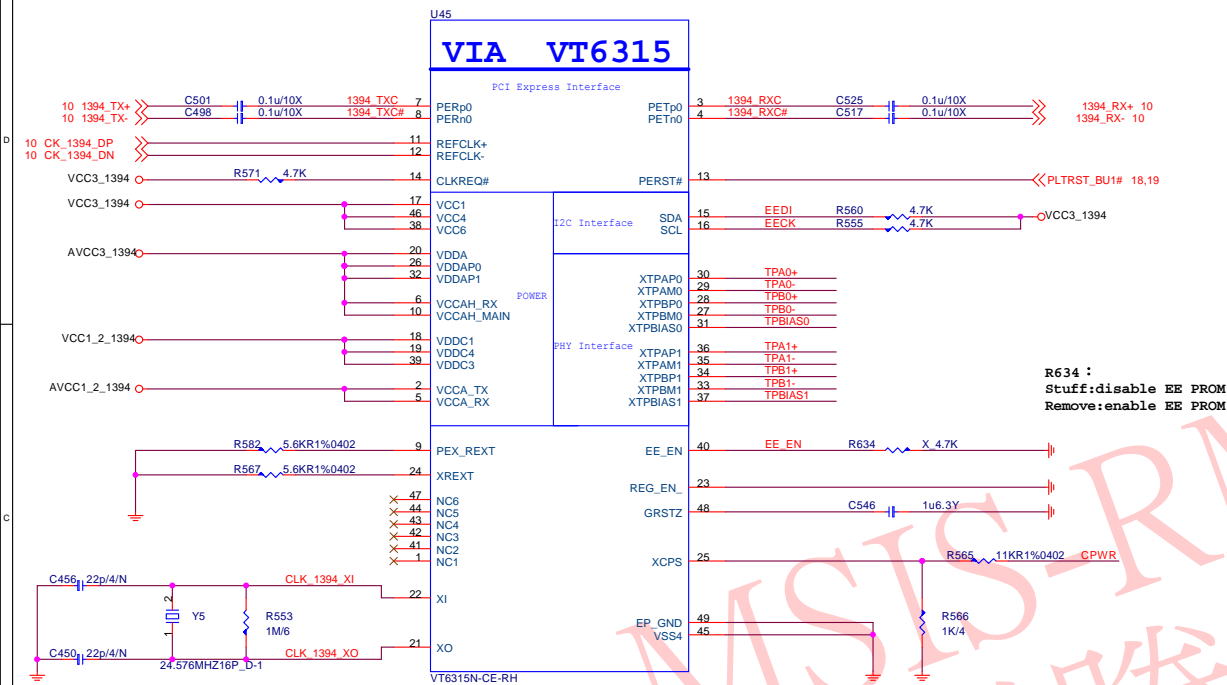


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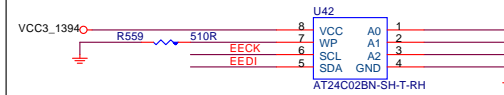
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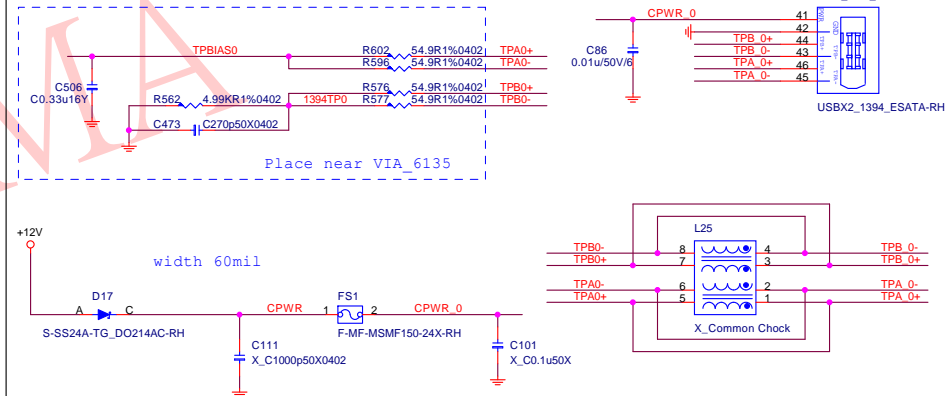
1394 CONTROLLER



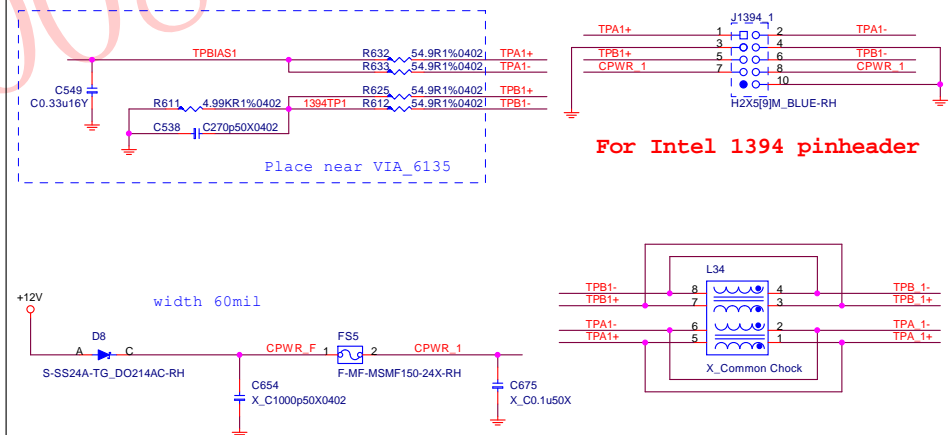
EE PROM



Rear 1394 port



Front 1394 pin header



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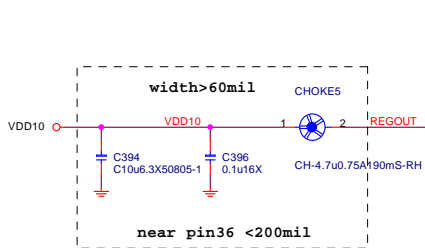
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RTL8111E Giga LAN

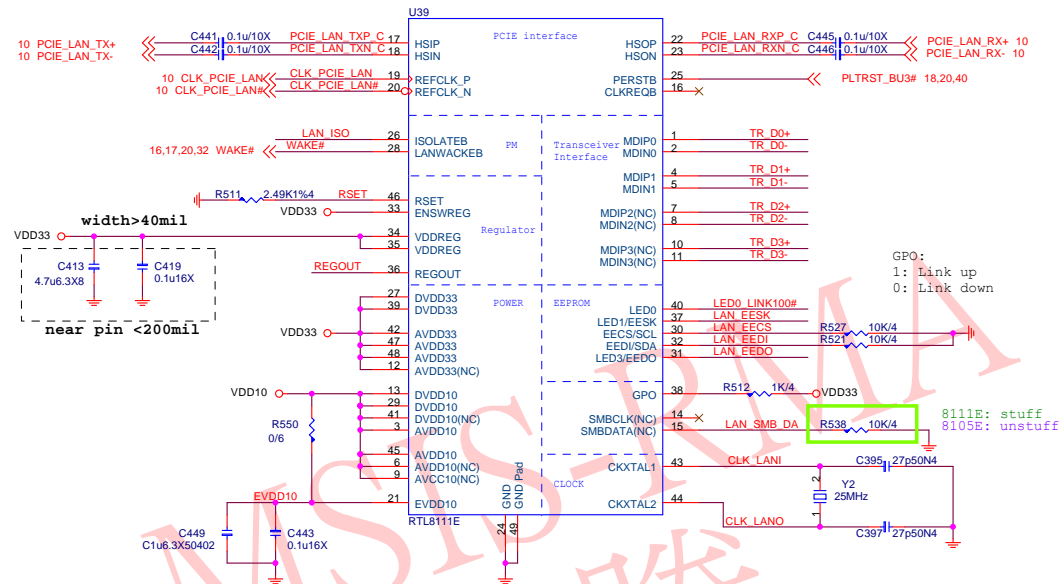
RTL8105E 10/100M LAN



ENSWREG:
1: Enable switching regulator
0: Disable switching regulator

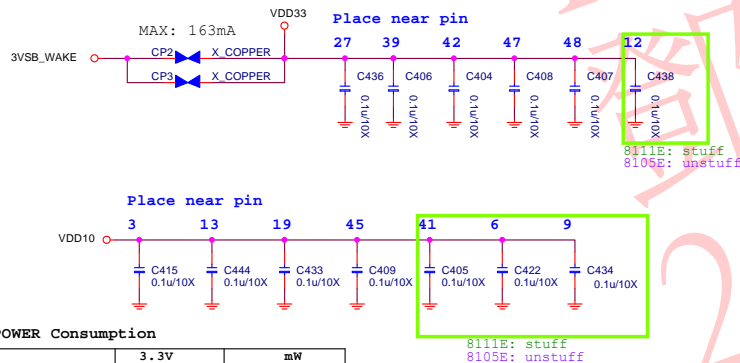


CHOKES (>0.6A) AVL:
L04-22A7470-T04
L04-47A7340-T04
L04-47A7330-T04
L04-47A7320-T04



Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

3.3v Power on rise time : 1~100ms.

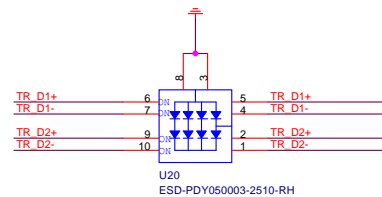


8105E POWER Consumption

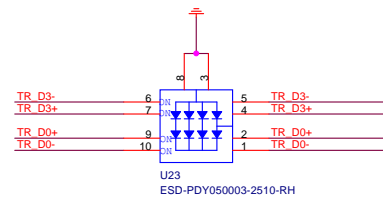
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

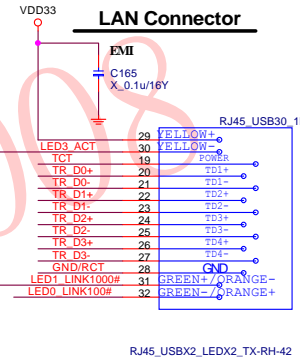
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



close to Connector

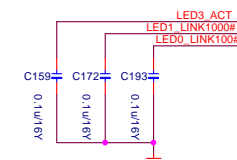


close to Connector



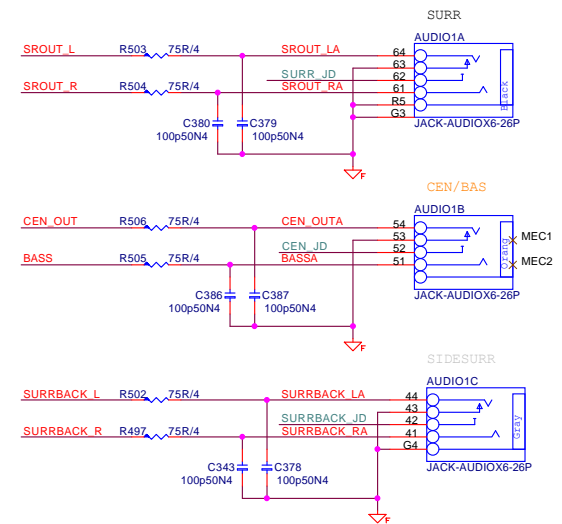
only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

Giga-Lan	10/100-Lan
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None	N58-22F0771 Link Yellow Active Blinking 1000 Orange 100 Green 10 None
19 20 21 22	19 20 21 22



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ALC892



HDA_RESET#

VCC3

R235
10K

X

Q66
2N7002

Y

Z

R749
10K/4

VCC3

PRSNT2_#

R817
X 0/4

R133
4.7K

D48
S-BAT54A_SOT23

VCC3

HDA_DISABLE#

HDA_RESET#

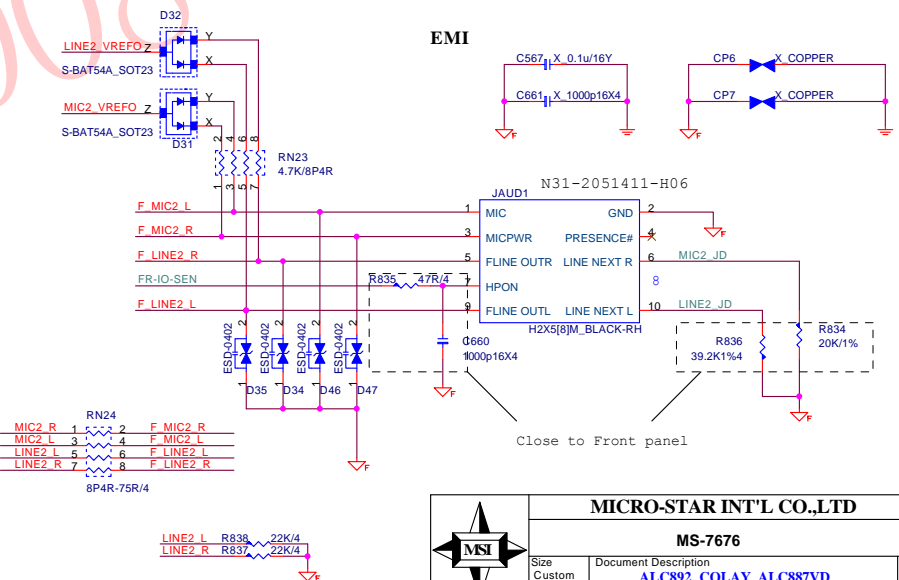
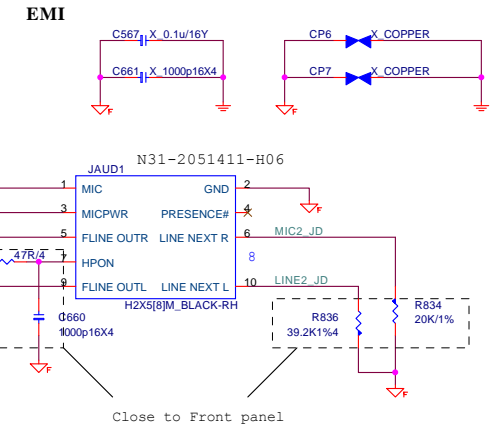
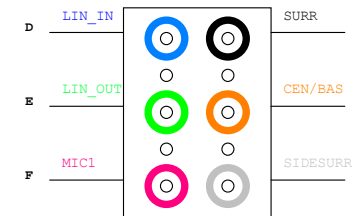
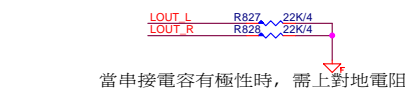
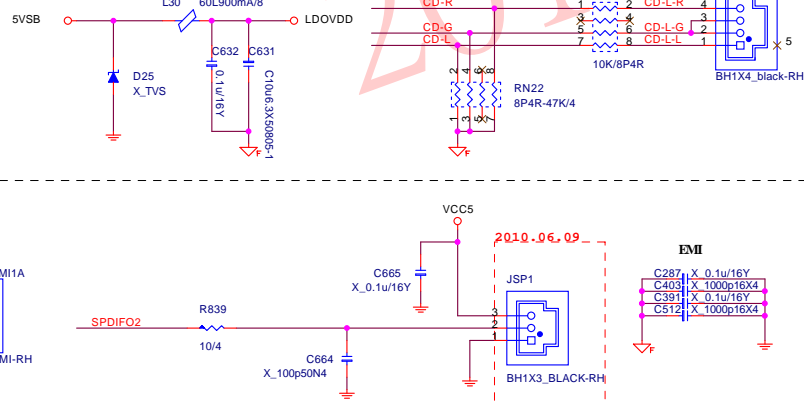
18 HDA_DISABLE# >>

12 AZ_RST# >>

16 PRSNT2# >>

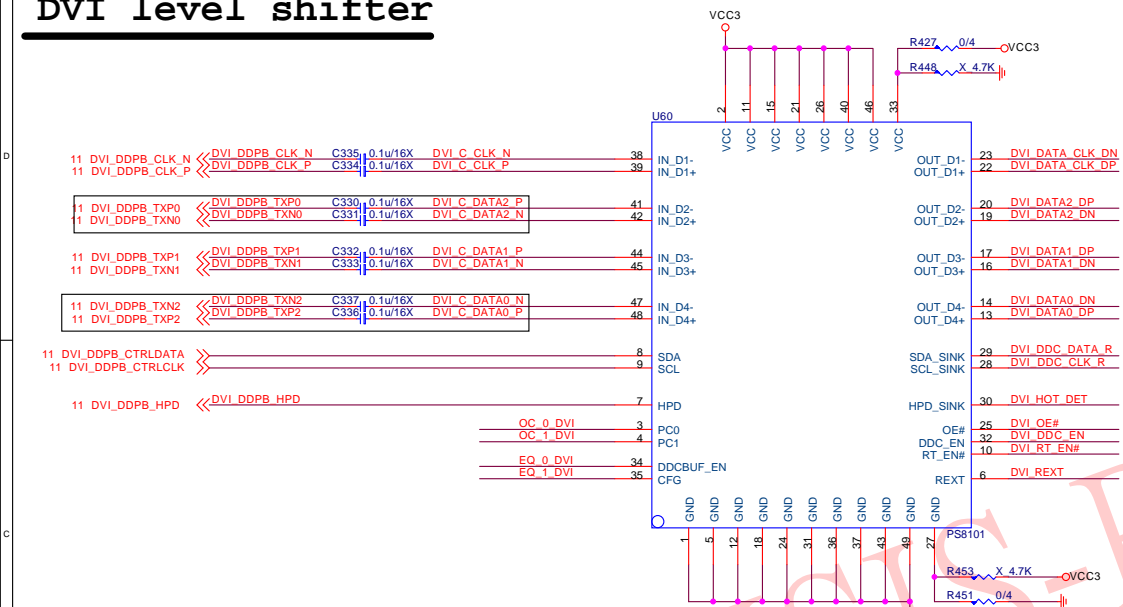
16 PE_GND << PE_GND to SIO GPI pin

Hi: onboard codec Verb table
Low: PCIe Audio Verb table



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MS-7676			
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DVI level shifter

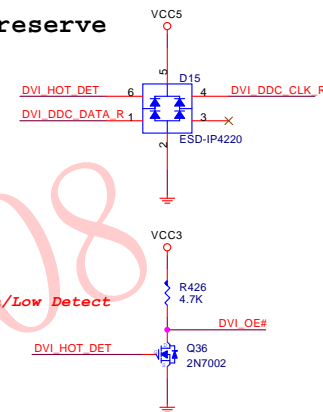


PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.

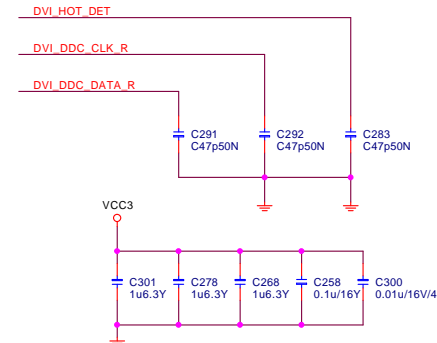
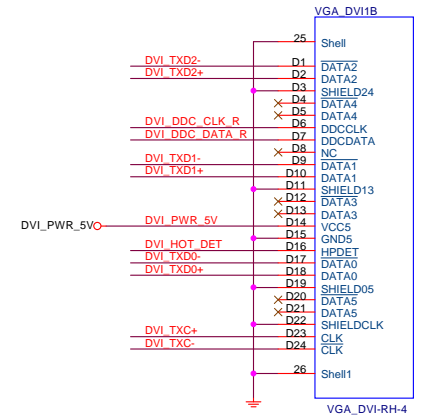
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPDP	DDSP_B_HPDP0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_CTRL_DATA	

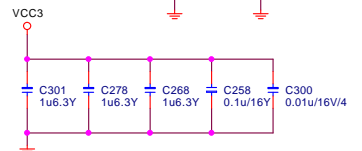
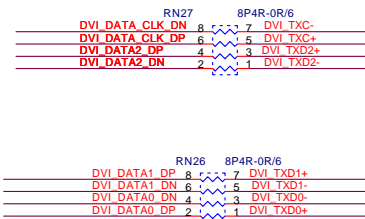
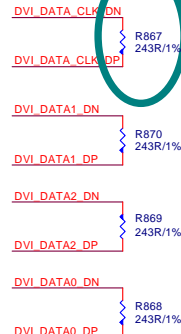
reserve



注: High/Low Detect



EMI



MICRO-STAR INT'L CO., LTD

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	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	note
1, 0, X	On	Off	internal pull-down at ~500K ohm.
1, 1, 0	Off	On	
1, 1, 1	Off	Off	
0, X, X	Off	Off	

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

HDMI level shifter

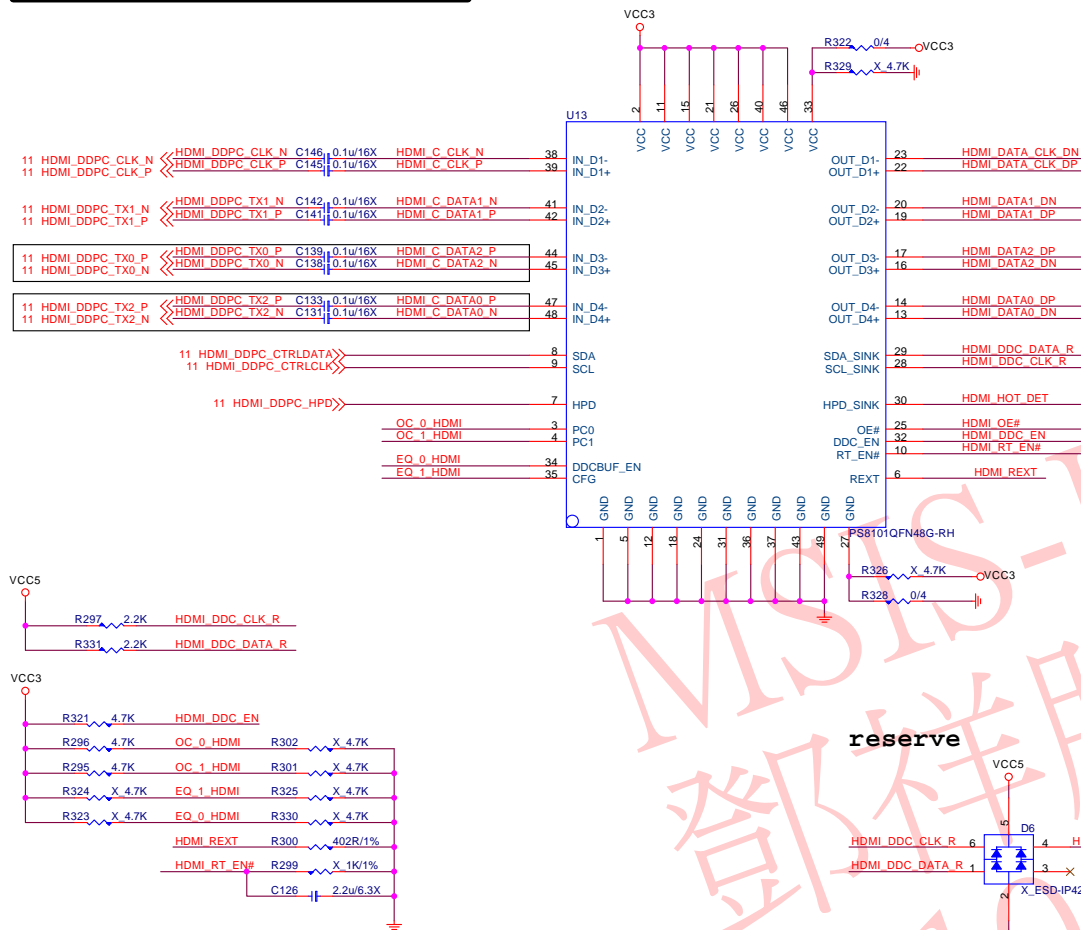
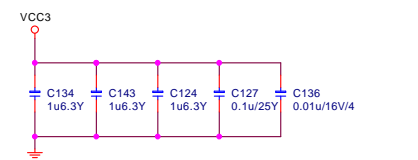
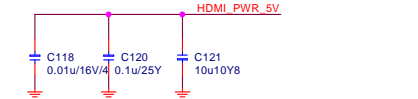
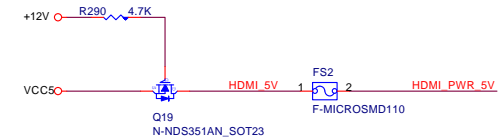
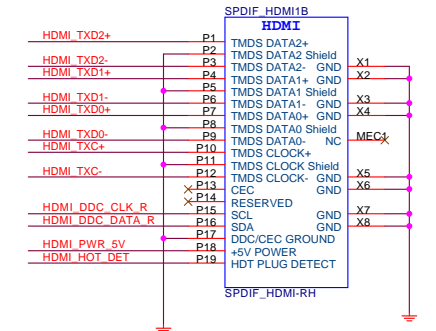


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

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Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI8_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI8_CTRL_DATA	



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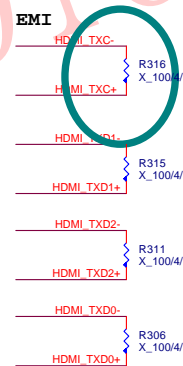
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Custom	HDMI	10

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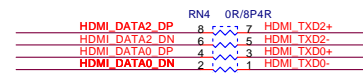
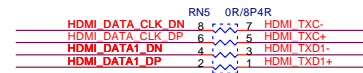
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

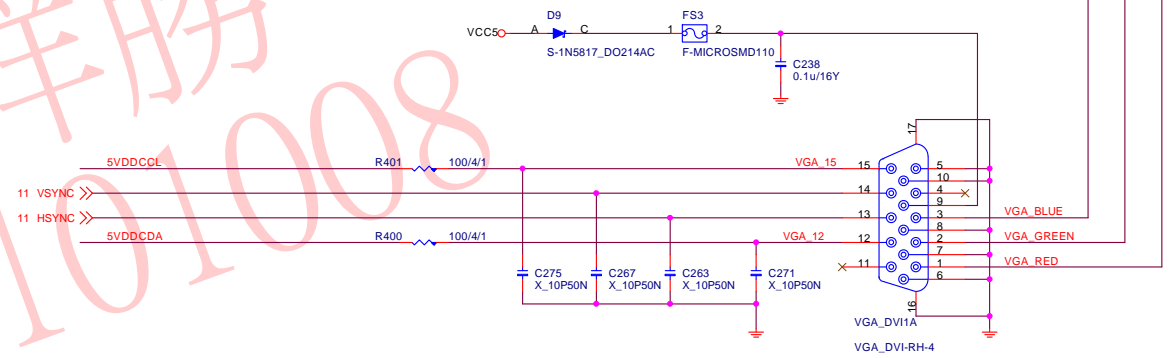
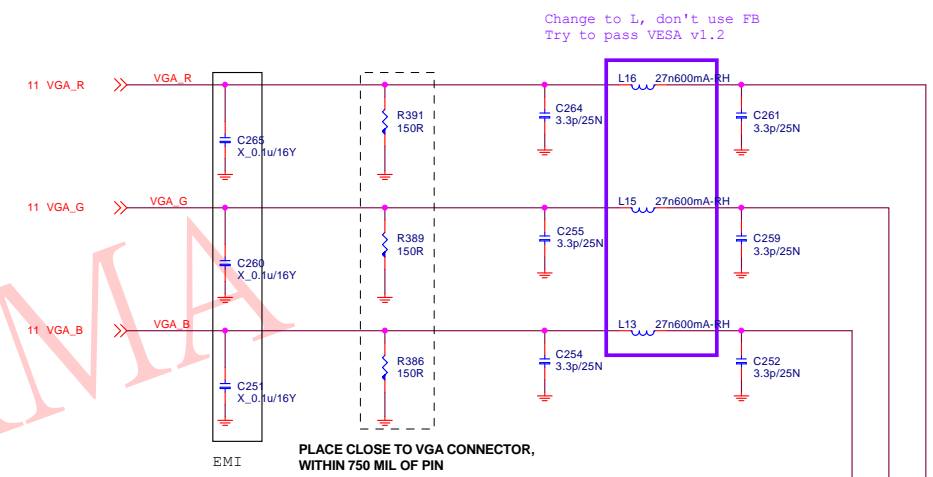
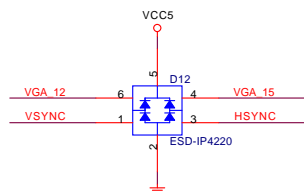
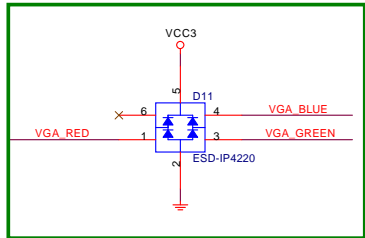
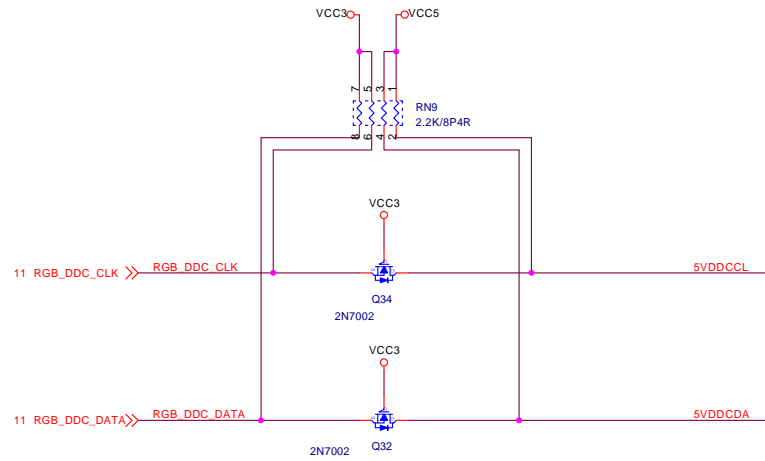


注 NHigh/Low Detect

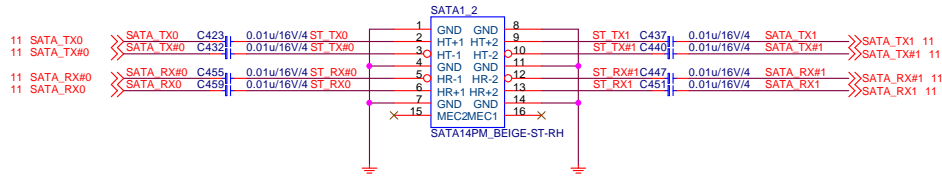


D-Sub

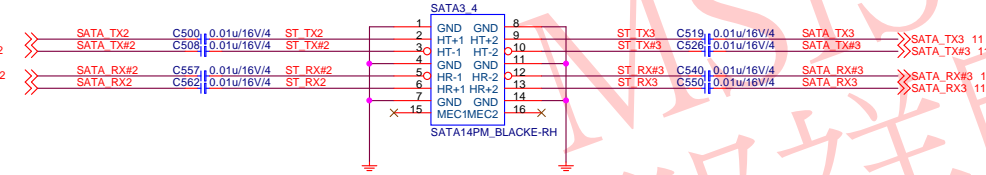
Level shift



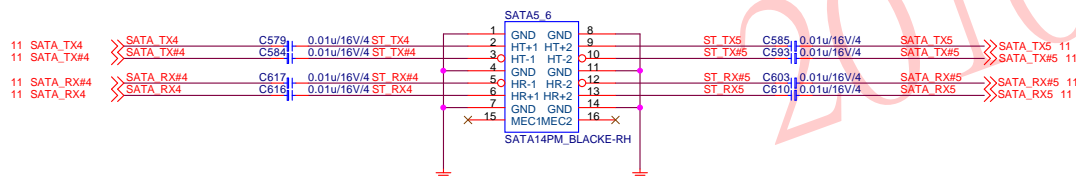
SATA 6G PORT 0,1



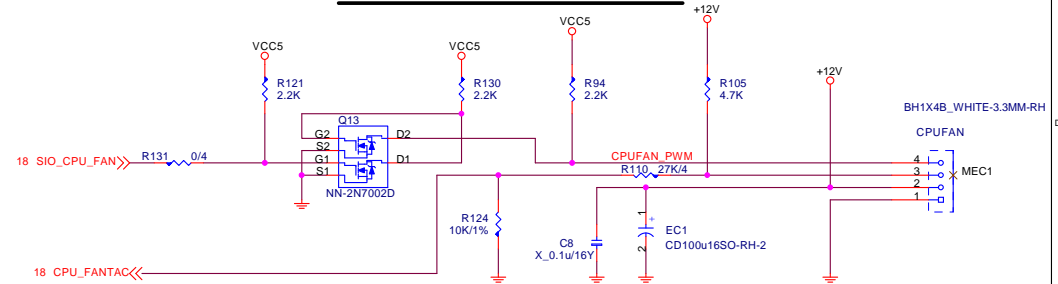
SATA 3G PORT 2,3



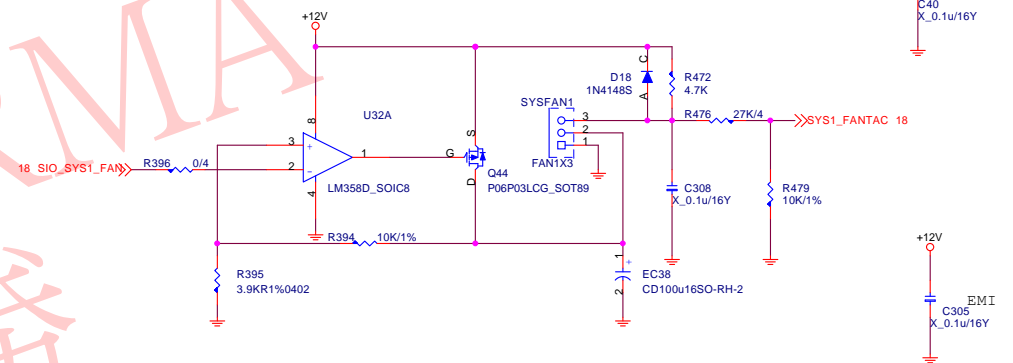
SATA 3G PORT 4,5



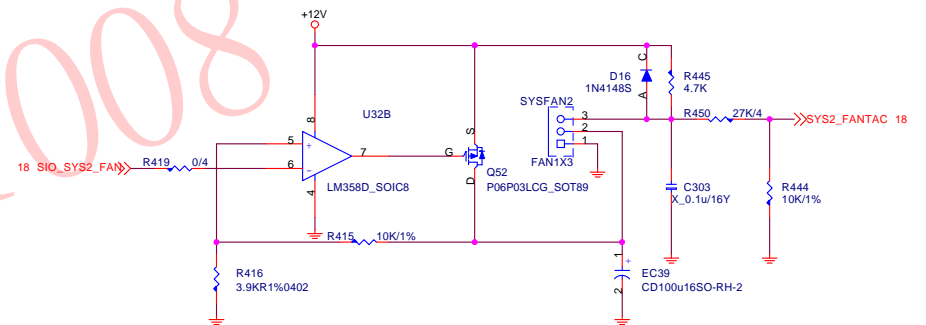
CPU FAN-COUNTROL CIRCUIT



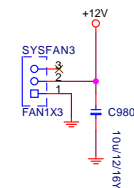
SYSTEM FAN1-COUNTROL CIRCUIT



SYSTEM FAN2-COUNTROL CIRCUIT

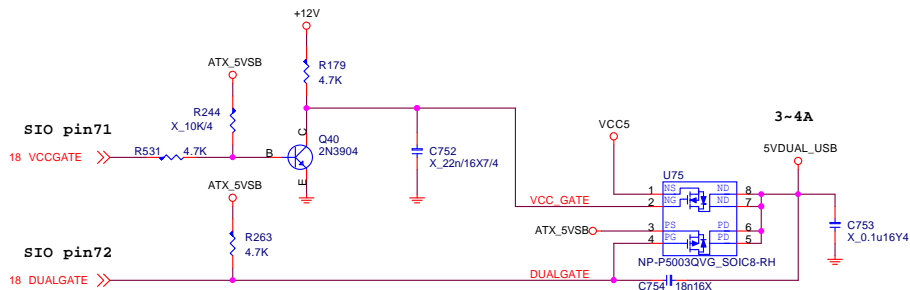


SYSTEM FAN3-12V



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5VDUAL_USB



SIO GPIO40 Pin7 (I_VSB3V)

USB_CHARGE: (OD)

0: Don't support USB charge and resume.
1: Support USB charge and resume.

Power plug in , H/W default support USB charge.

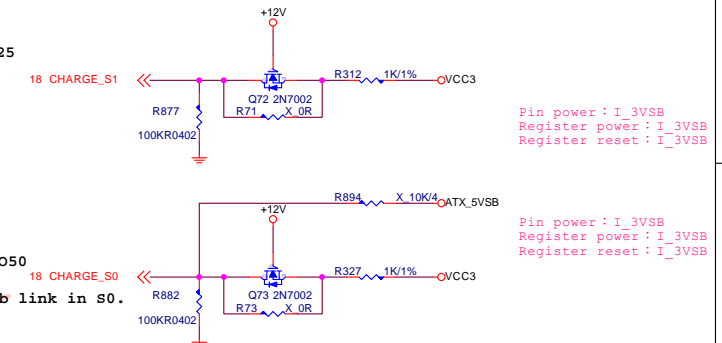
SIO GPIO25 (I_VSB3V)
SIO GPIO50 (I_VSB3V)

CHARGE_S1: (PUSH PULL)
CHARGE_S0: (PUSH PULL)

	S0	S1
AUTO:	0	0
DCP :	0	1
A :	1	0
Y :	1	1

SIO GPIO40

18 USB_CHARGE >>> R18 OR CHARGE_EN
18,20,21,30 USB_MODE >>> R64 X OR

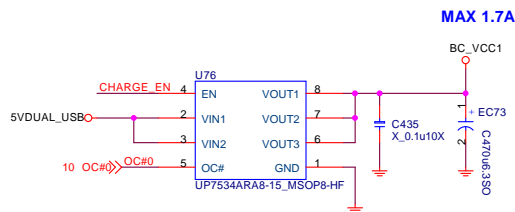


Pin power : I_3VSB or VBAT
Register power : I_3VSB or VBAT
Register reset : I_3VSB or VBAT

Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB

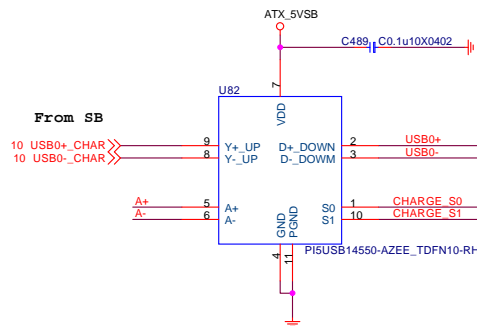
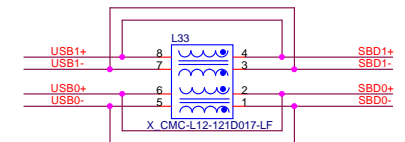
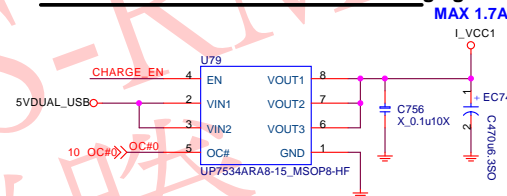
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB

USB POWER FOR PORT 0 for USBCharging

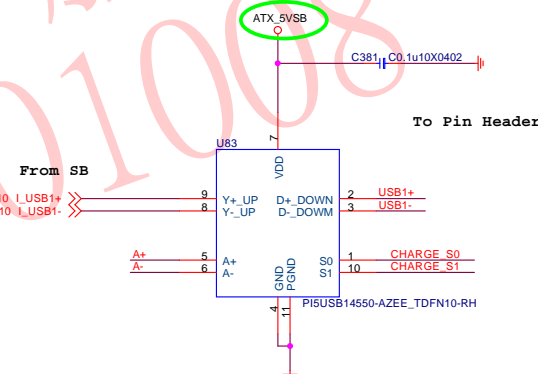


H/W default support auto charging in S3/S4/S5 and usb link in S0.

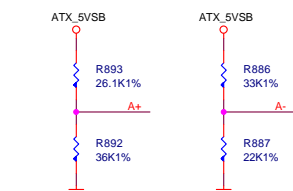
USB POWER FOR PORT 1 for USBCharging



S1	0	0	1
S0	0	1	1
Mode	AUTO	A	Y



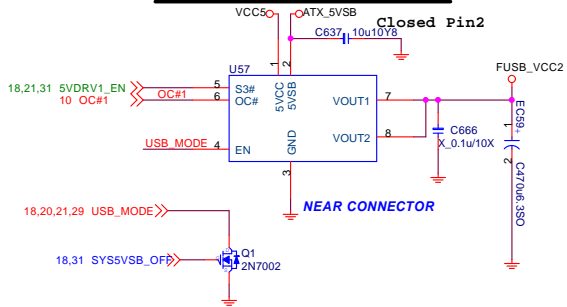
PI5USB14550 has internal EDS diode.



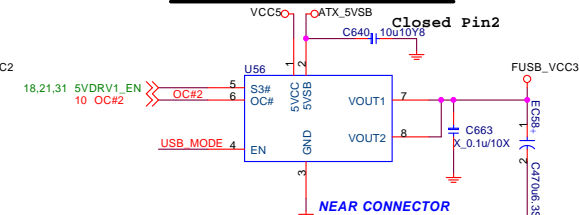
D+ pull High 2.75 V
D- pull High 2.05V
皆可對 i-Pad / i-Phone / i-Pod進行充電。

Front USB Connector

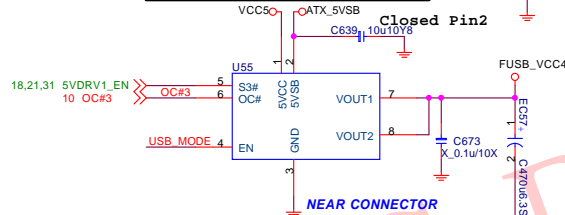
USB POWER REAL PORT 2,3



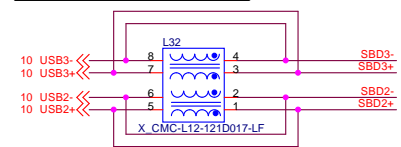
USB POWER FOR PORT 4,5



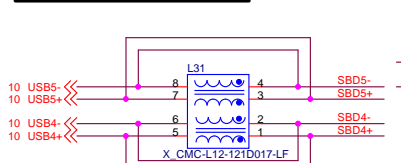
USB POWER FOR PORT 6,7



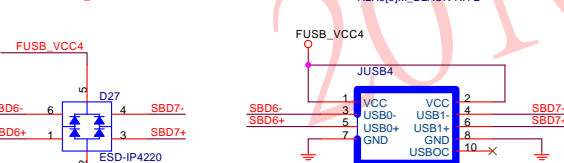
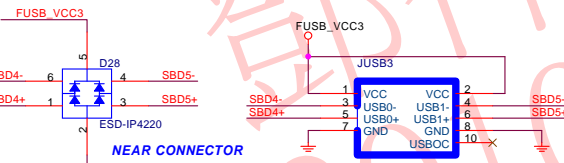
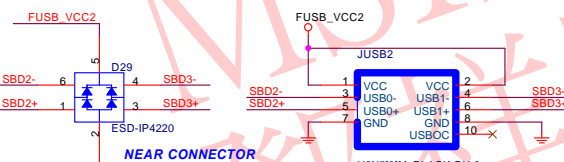
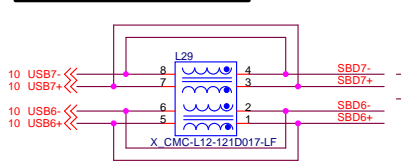
FRONT USB PORT 2,3



FRONT USB PORT 4,5

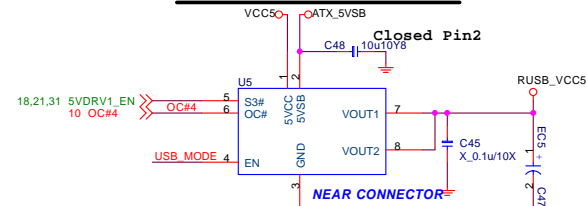


FRONT USB PORT 6,7

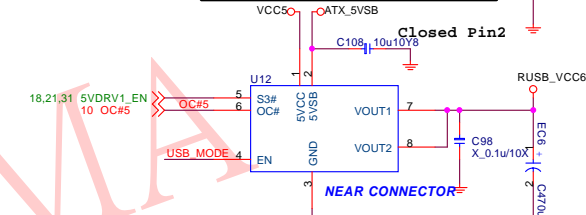


Rear USB Connector

USB POWER FOR PORT 6,7

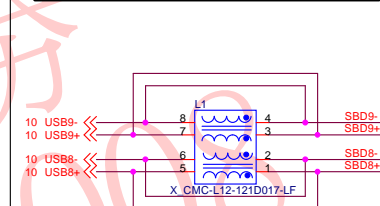


USB POWER FOR PORT 8,9

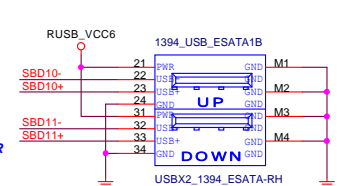
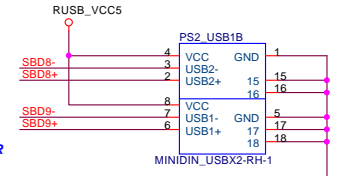
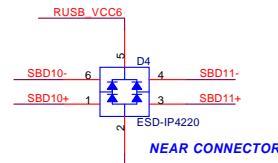
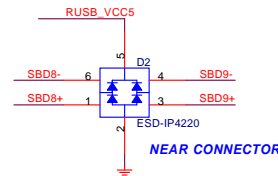
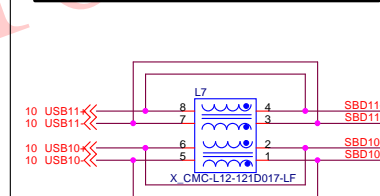


USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

REAR USB PORT 8,9 (With PS2)



REAR USB PORT 10,11 (With 1394)

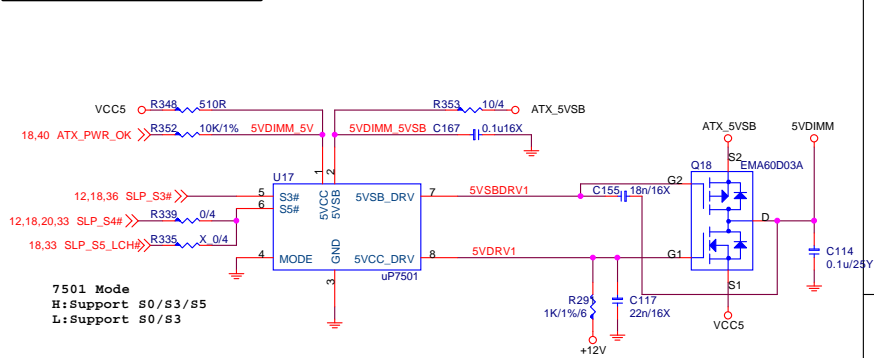


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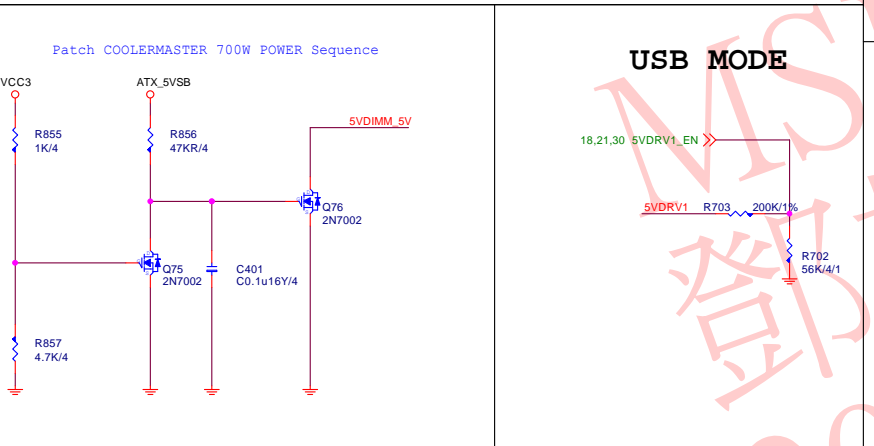
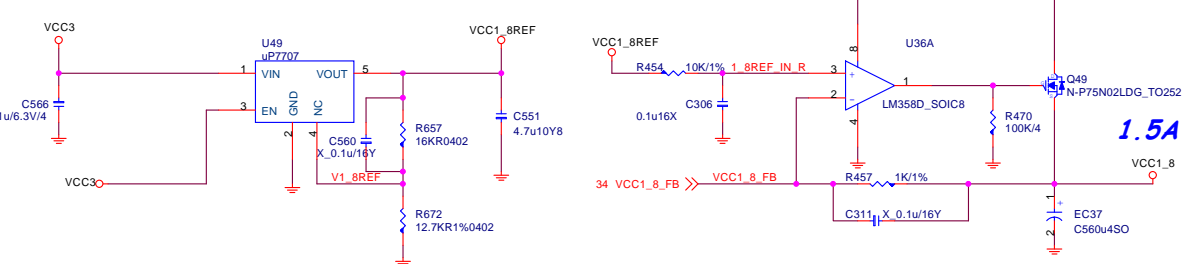
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Size	Document Description	Rev
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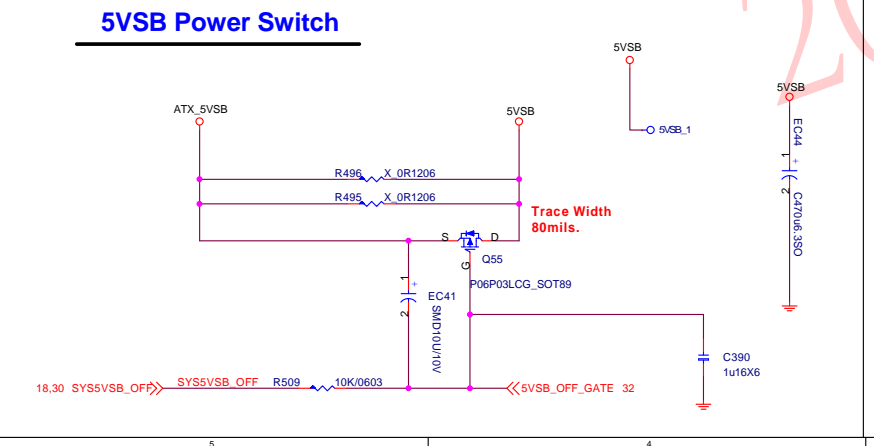
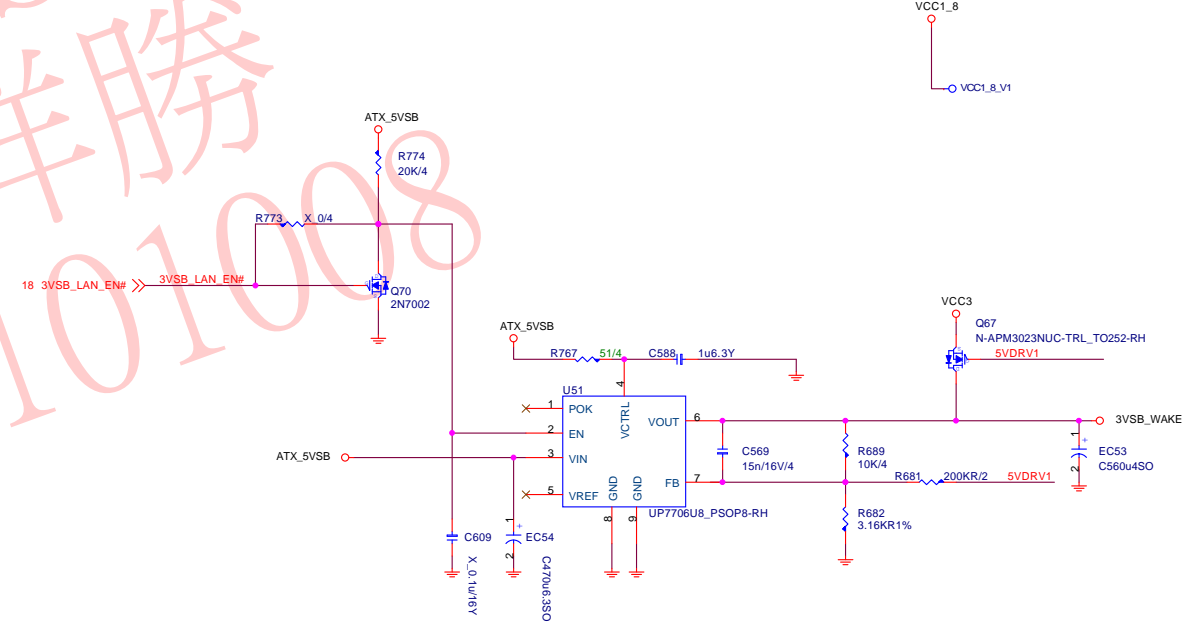
5VDIMM FOR DDR



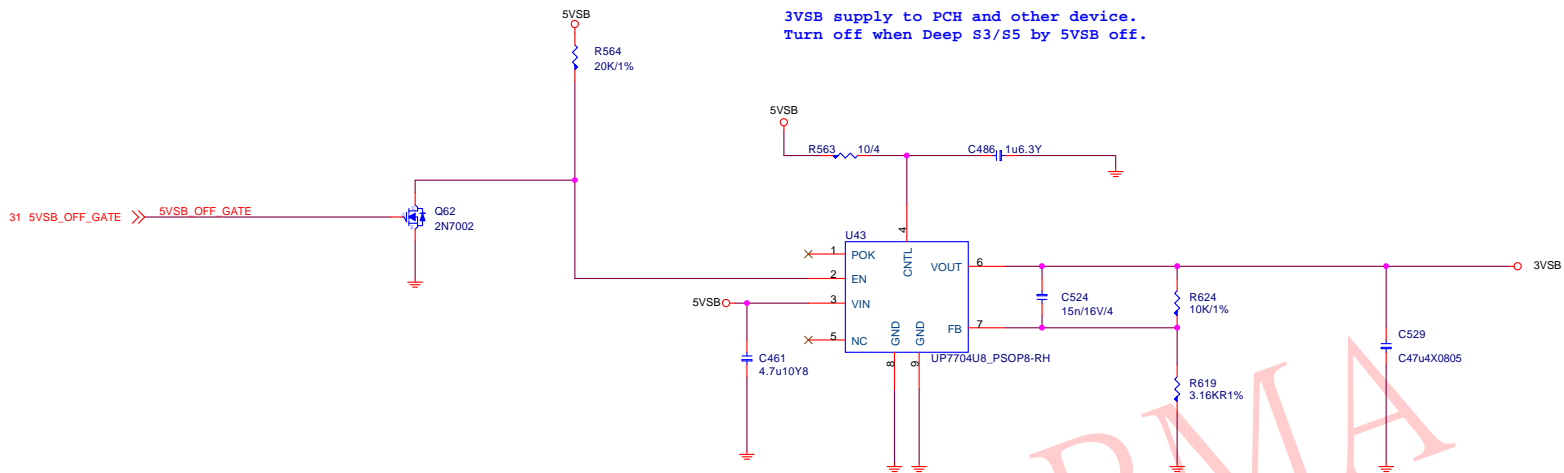
VCC1_8REF



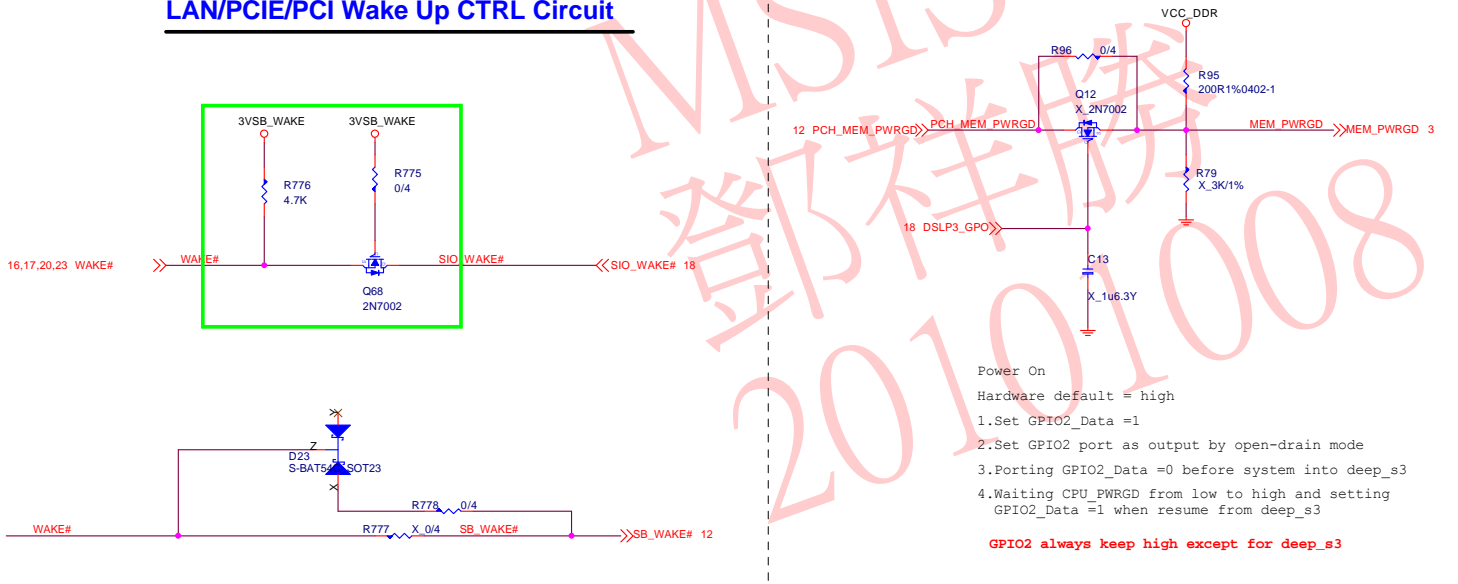
3VSB_WAKE



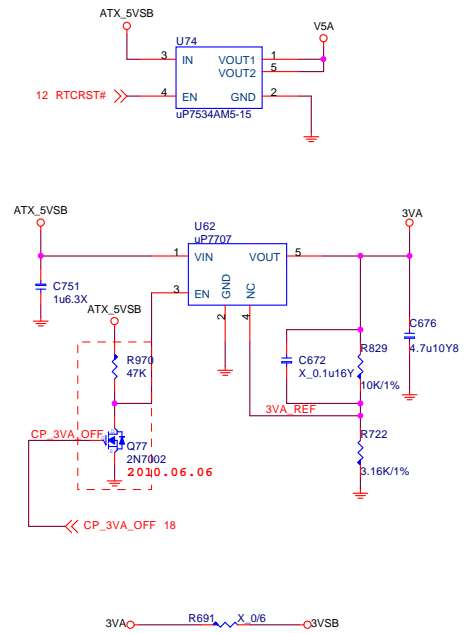
Deep Mode WOL LAN Power CTRL Circuit



LAN/PCIE/PCI Wake Up CTRL Circuit



RTCRST patch circuit for
clr-CMOS PCH will wake up issue



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DDR Power:1.5V

DDR3_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

SIO 出來是 0.9VREF

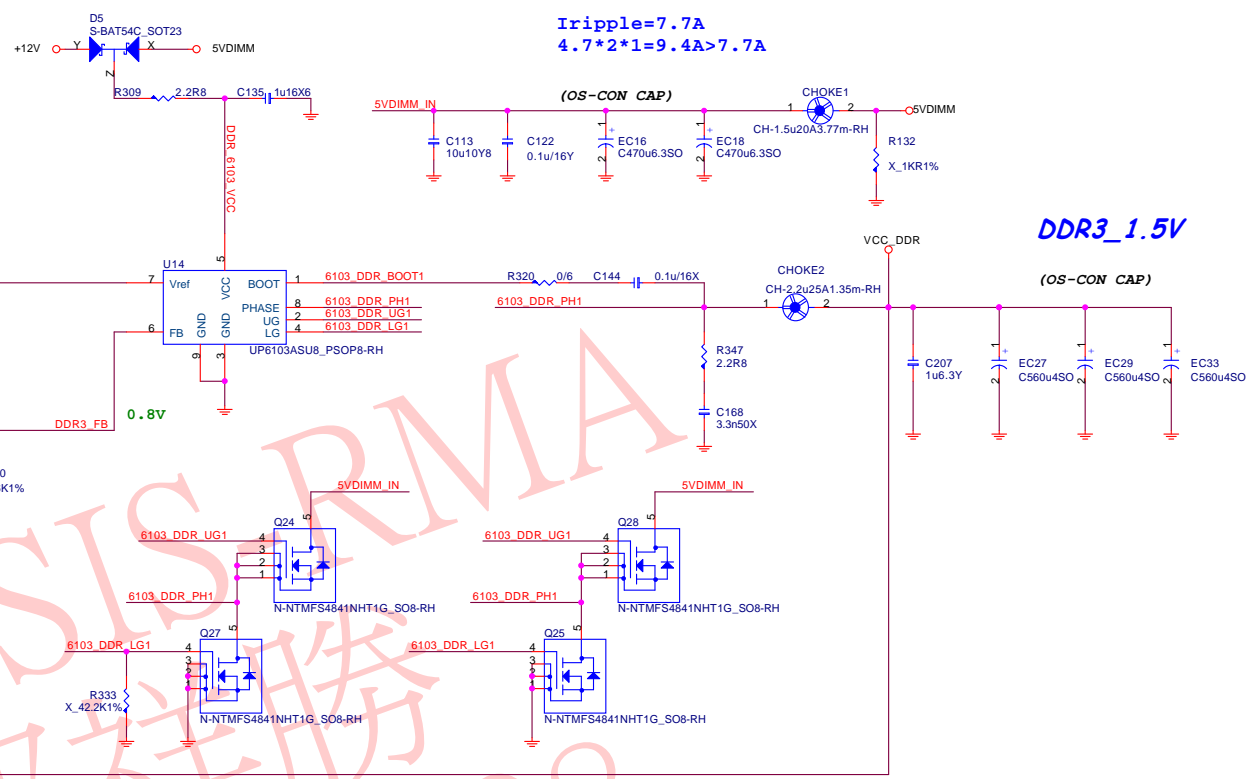
18 DDR_REF >> R308 1K/1% C140 0.1u/25V R313 8.06K/1%

DDR 0.9_REF_R

0.8V

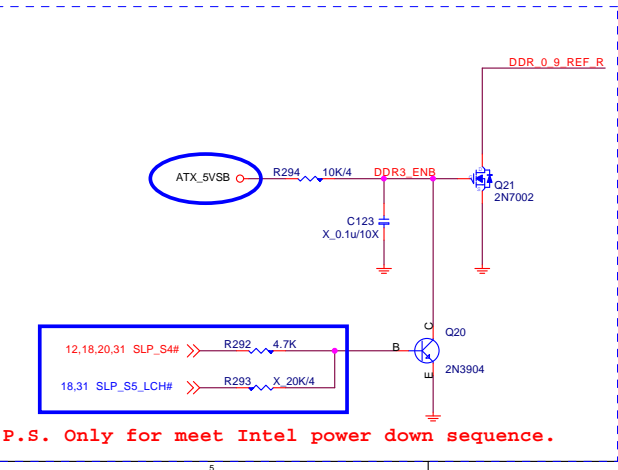
DDR3_FB

(0.9V*8.06K) / (1K+8.06K) = 0.795V
0.795V (1+ 7.15K/8.06K) = 1.5V (VCC_DDR)

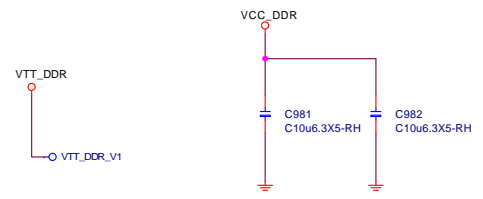
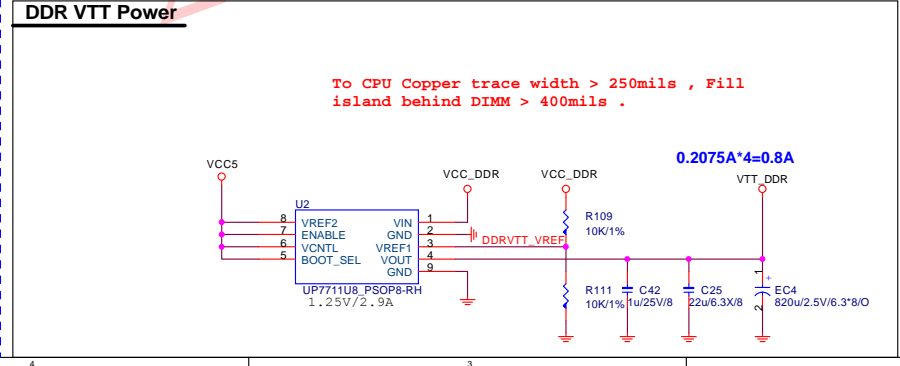


Iripple=7.7A
4.7*2*1=9.4A>7.7A

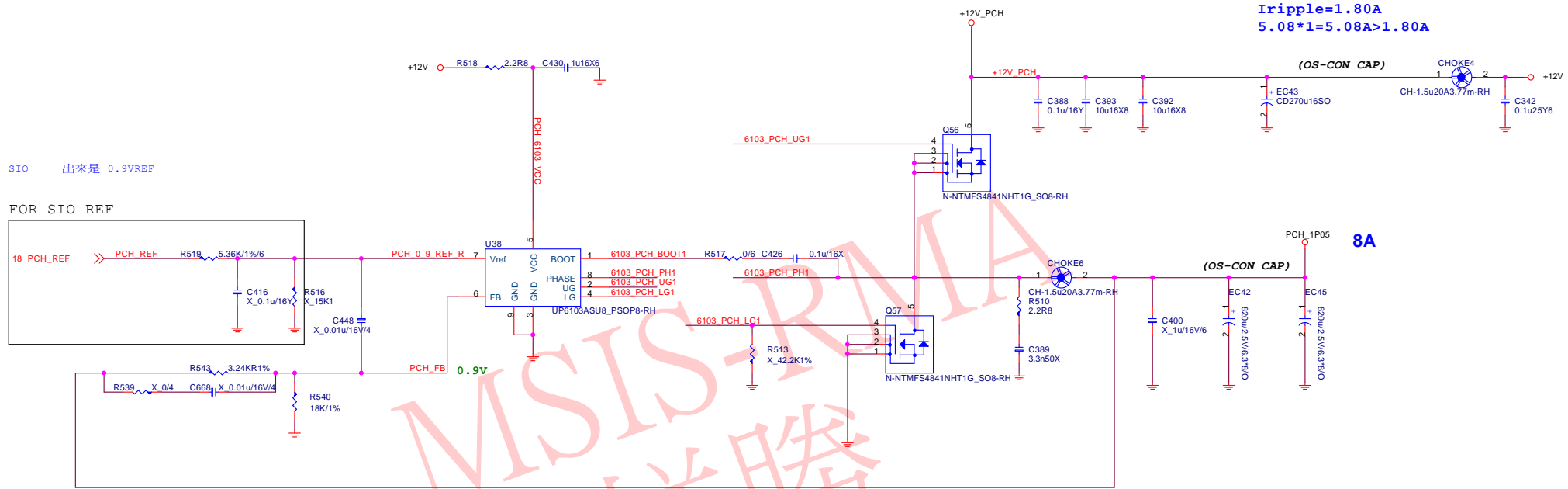
DDR3_1.5V



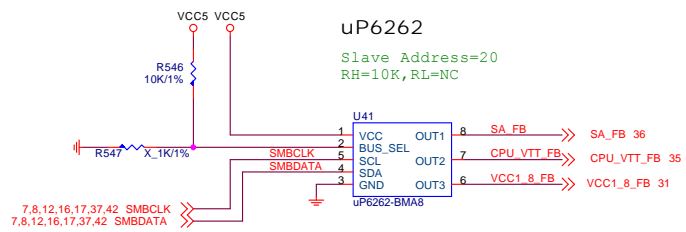
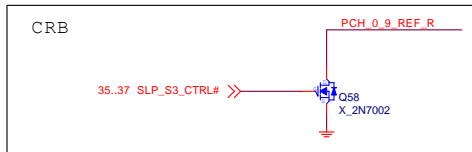
P.S. Only for meet Intel power down sequence.



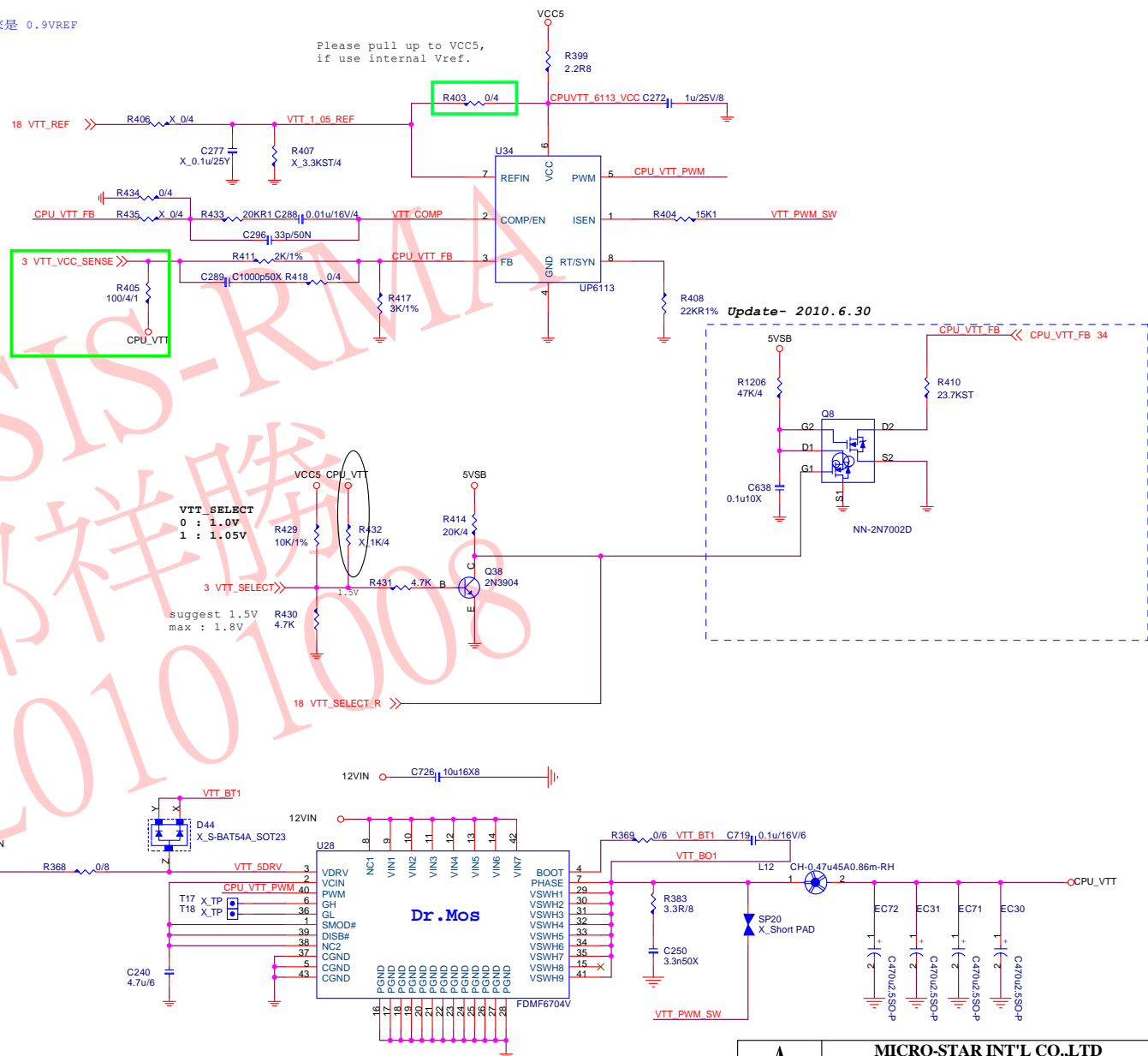
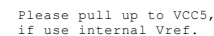
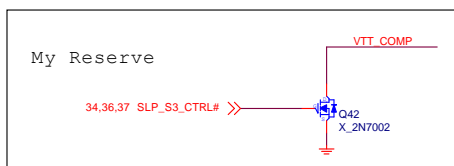
PCH Power:1.05V
PCH Core 6.2A+1.8A=8A
6.2A FOR PCH
1.8A FOR ME CORE



UPI VOLTAGE CONSOLE



8.5A FOR CPU



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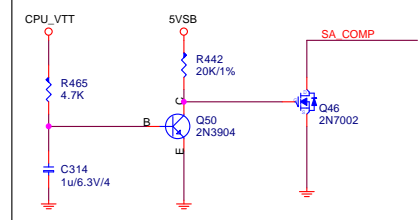
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Size Custom	Document Description CPU_VTT - uP6113- 1-Phase	Rev 10
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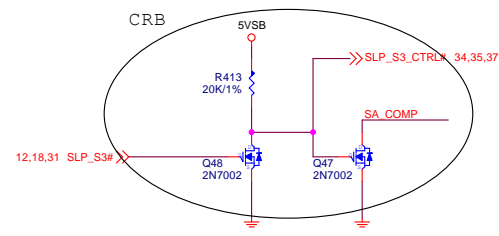
CPU_SA:0.925/0.85

SA Core =8.8A

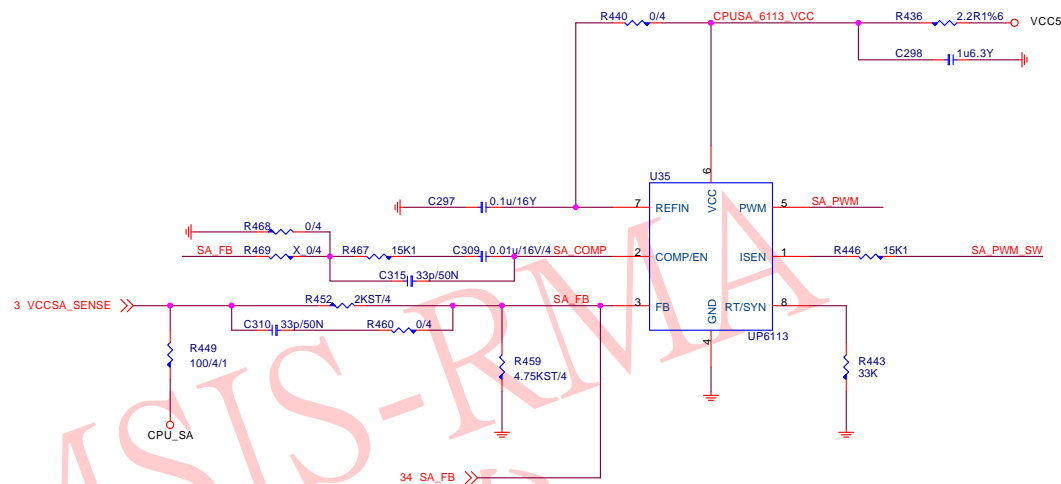
Waitting CPU_VTT Ready



CRB

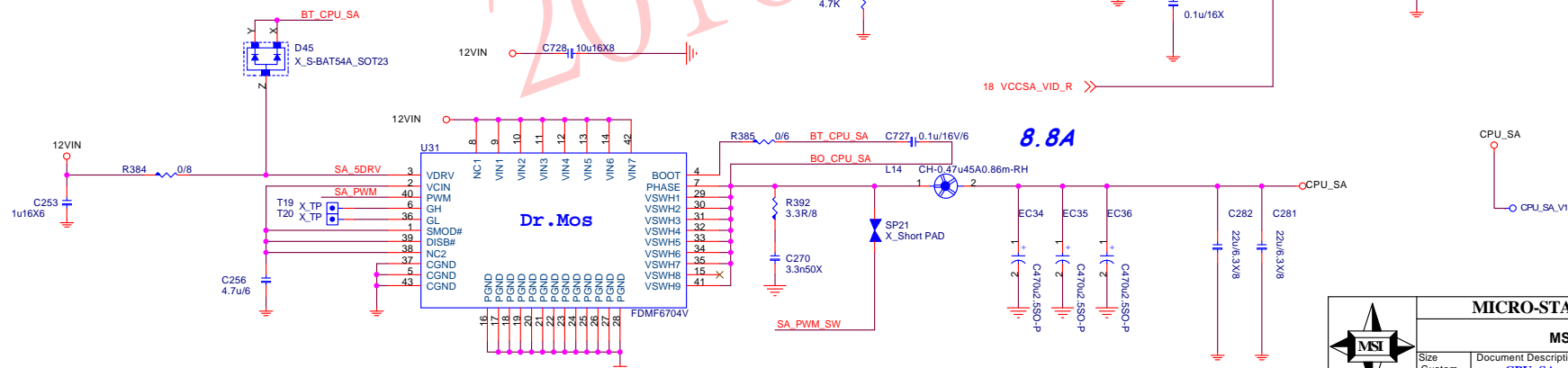


Please pull up to VCC5,
if use internal Vref.



VCCSA_VID
0 : 0.925V
1 : 0.85V

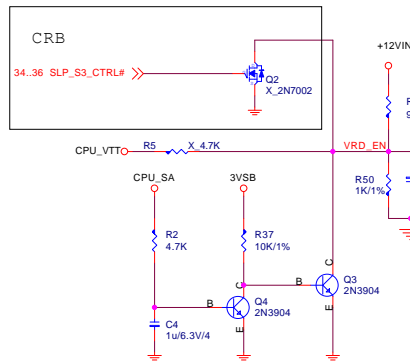
8.8A



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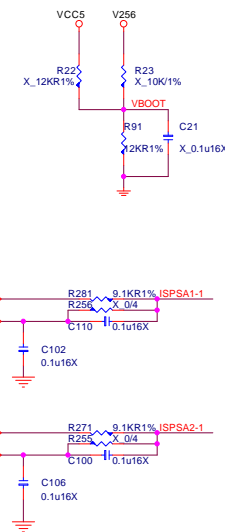
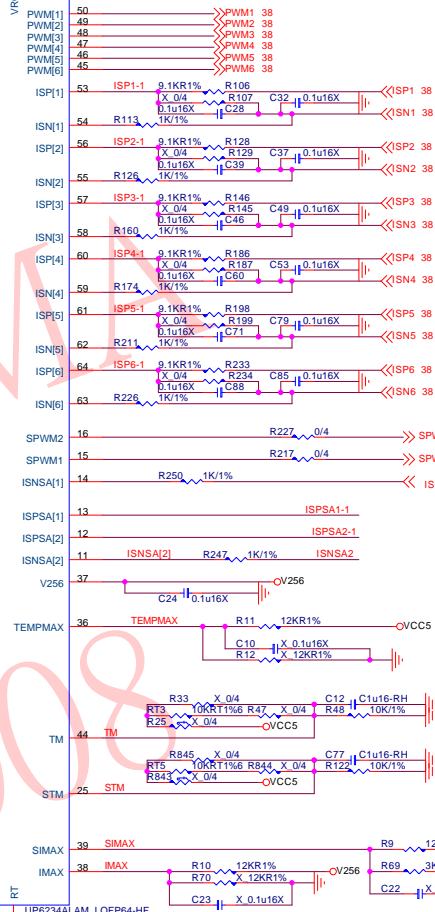
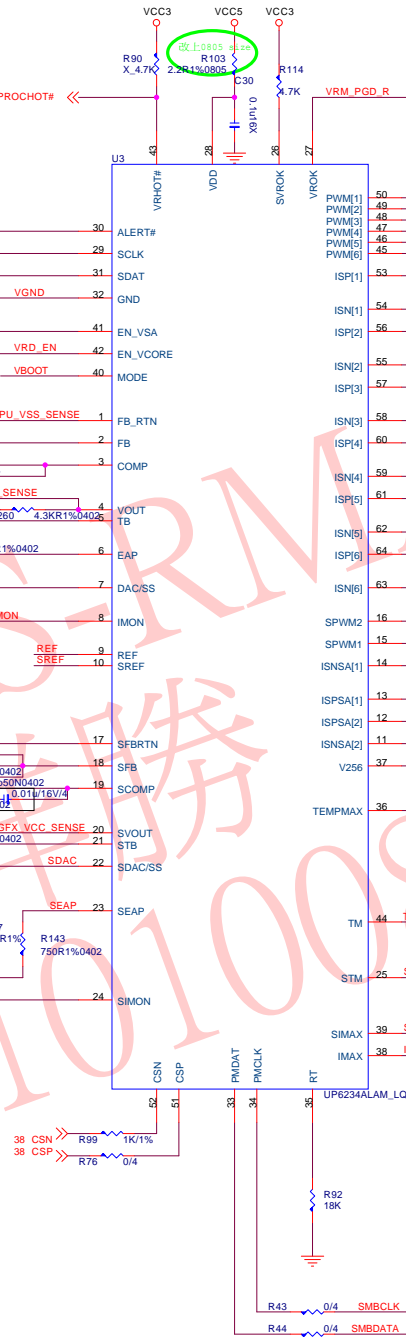
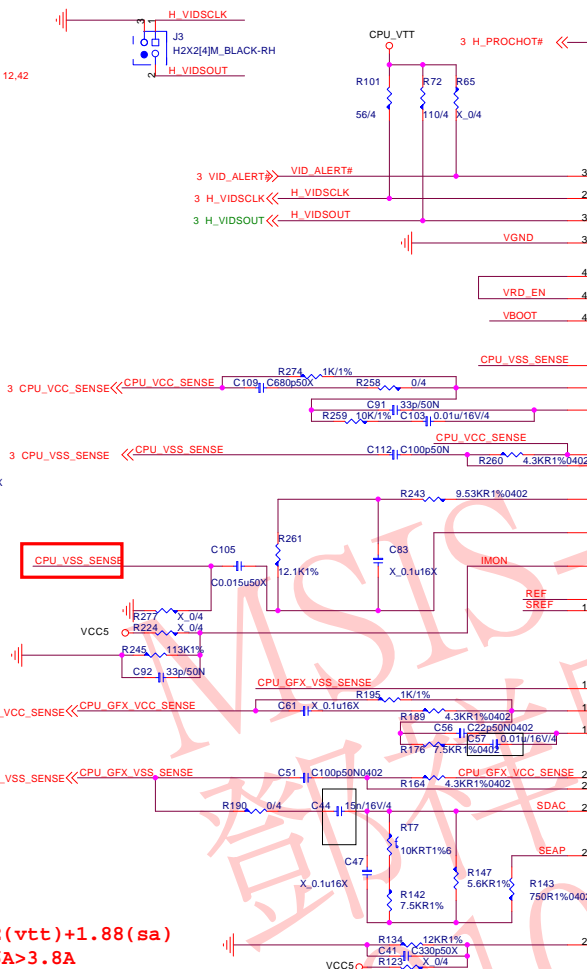
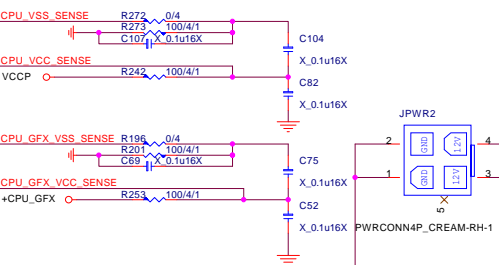
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Custom	CPU_SA - uP6113 1-Phase	10
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$$\text{Iriipple} = 1.92(\text{vtt}) + 1.88(\text{sa})$$

$$5.08 \times 2 = 10.16\text{A} > 3.8\text{A}$$

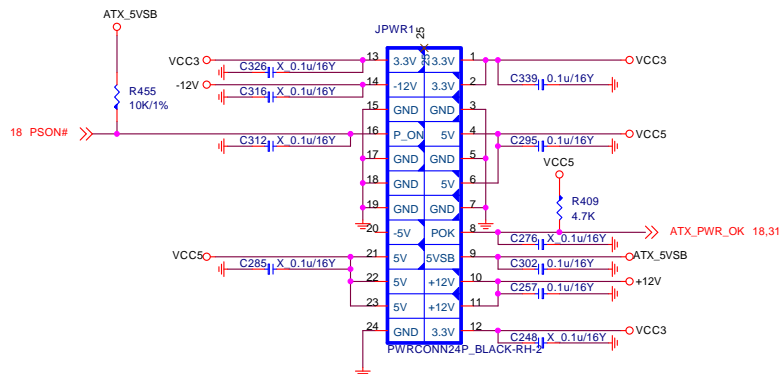


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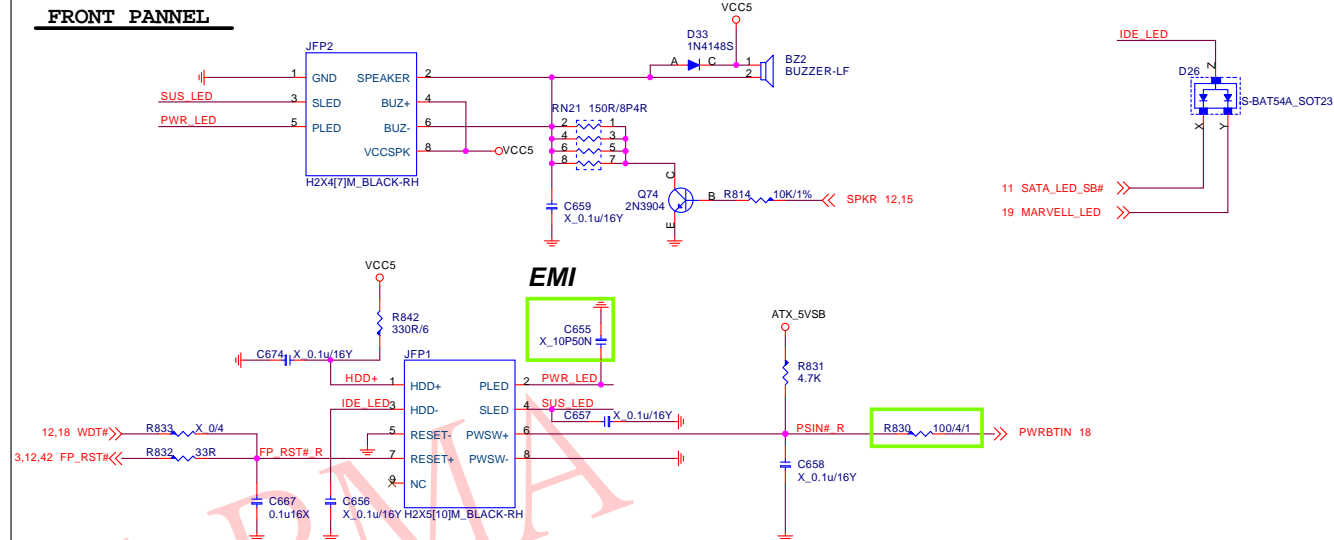
Rev
10

Custom	VRD12 - UPI6234 6+2-Phase	10
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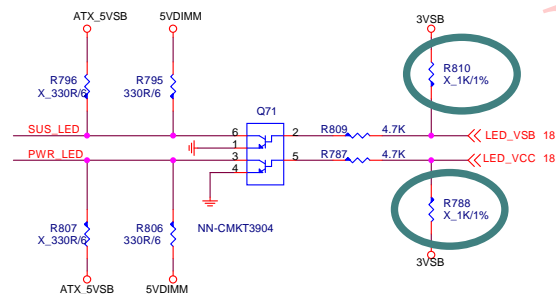
ATX POWER CONNECTOR



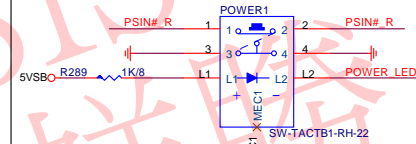
FRONT PANNEL



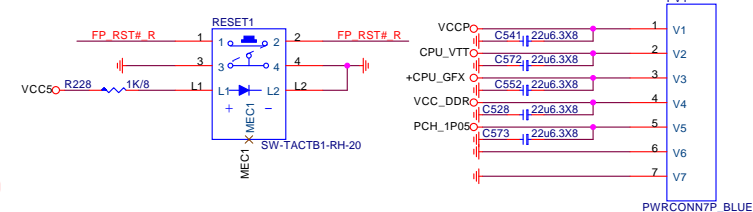
LED (for Fintek 71889)



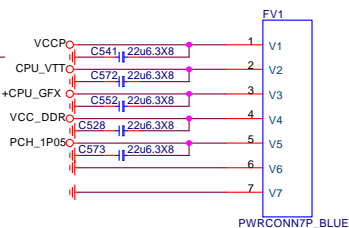
POWER ON BUTTON



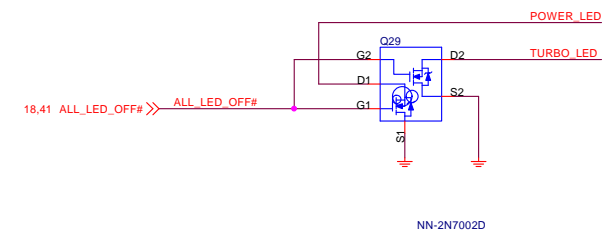
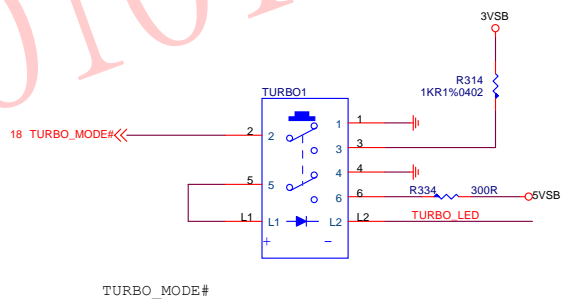
RESET BUTTON



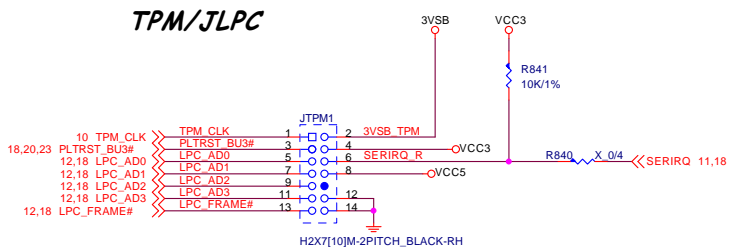
電壓測點



DPS Turbo Button



TPM/JLPC

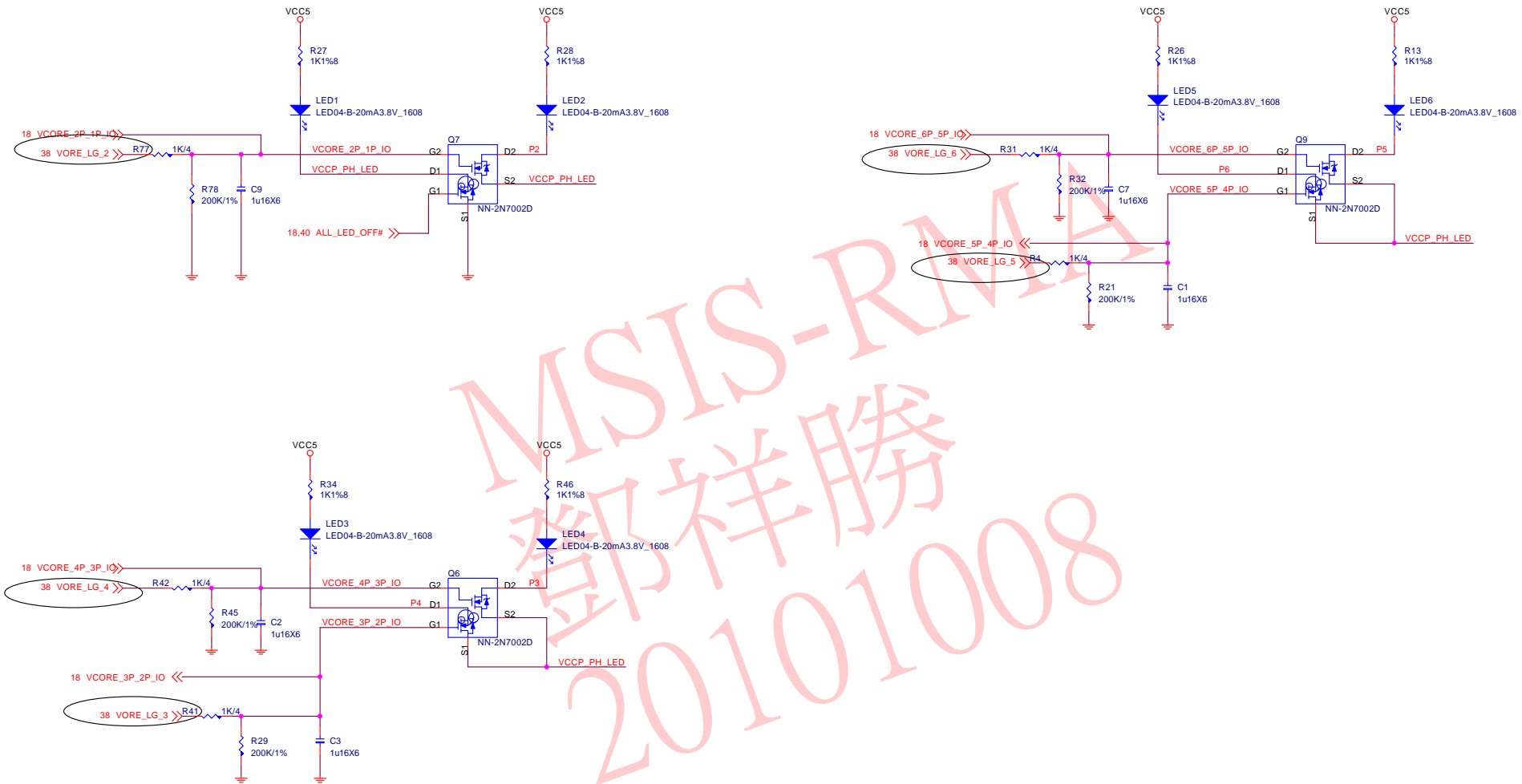


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all on board LED switch



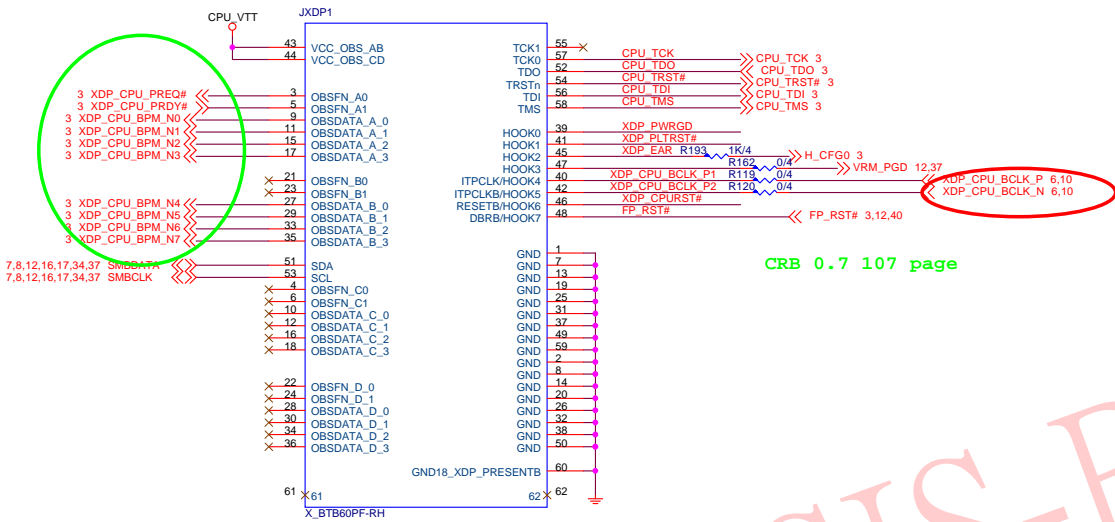
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Size Custom	Document Description PHASE Dropping & PSI & LED	Rev 10
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Reserve debug port 5020

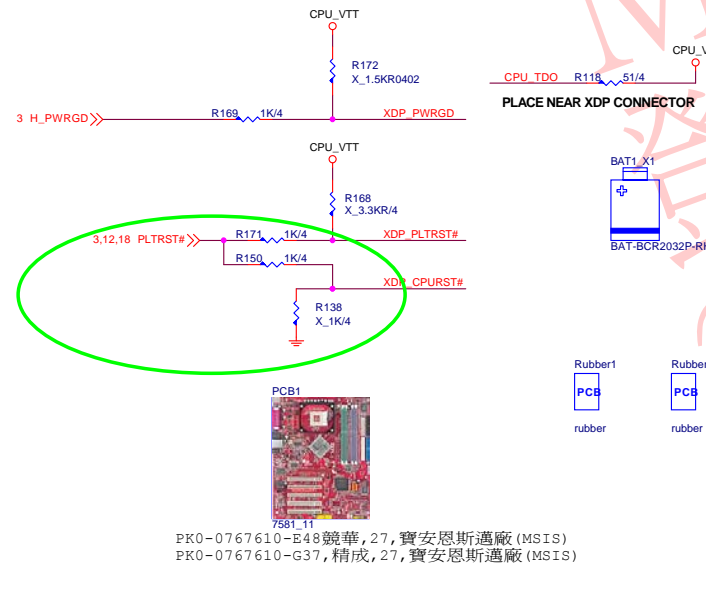
PCH XDP



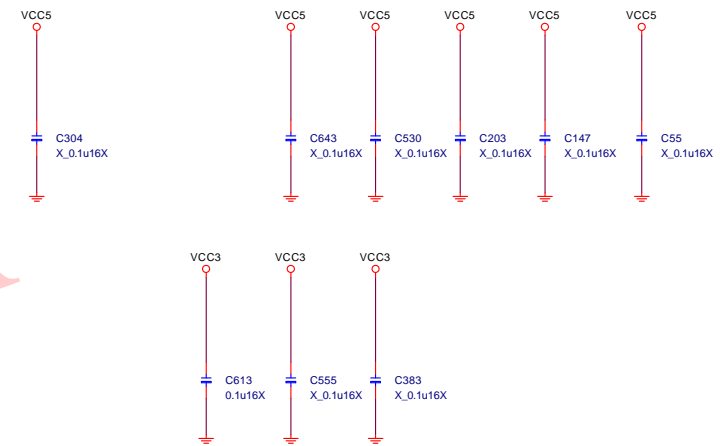
CRB 0.7 107 page

PCH XDP PWRGD/RESET

CPU Heat-pipe



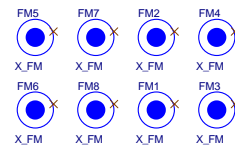
PK0-0767610-E48 競華, 27, 寶安恩斯邁廠 (MSIS)
PK0-0767610-G37, 精成, 27, 寶安恩斯邁廠 (MSIS)



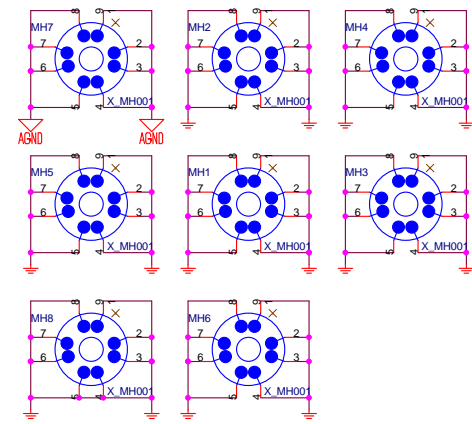
Simulation



Optical Fiducial Marks-120



Mounting Holes



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Custom	XDP / Manual Parts	10	
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